Cadence OrCAD X and Allegro X: What's New in Release 23.1

This document describes the new features and enhancements in Cadence® OrCAD® X and Allegro® X products in release 23.1.

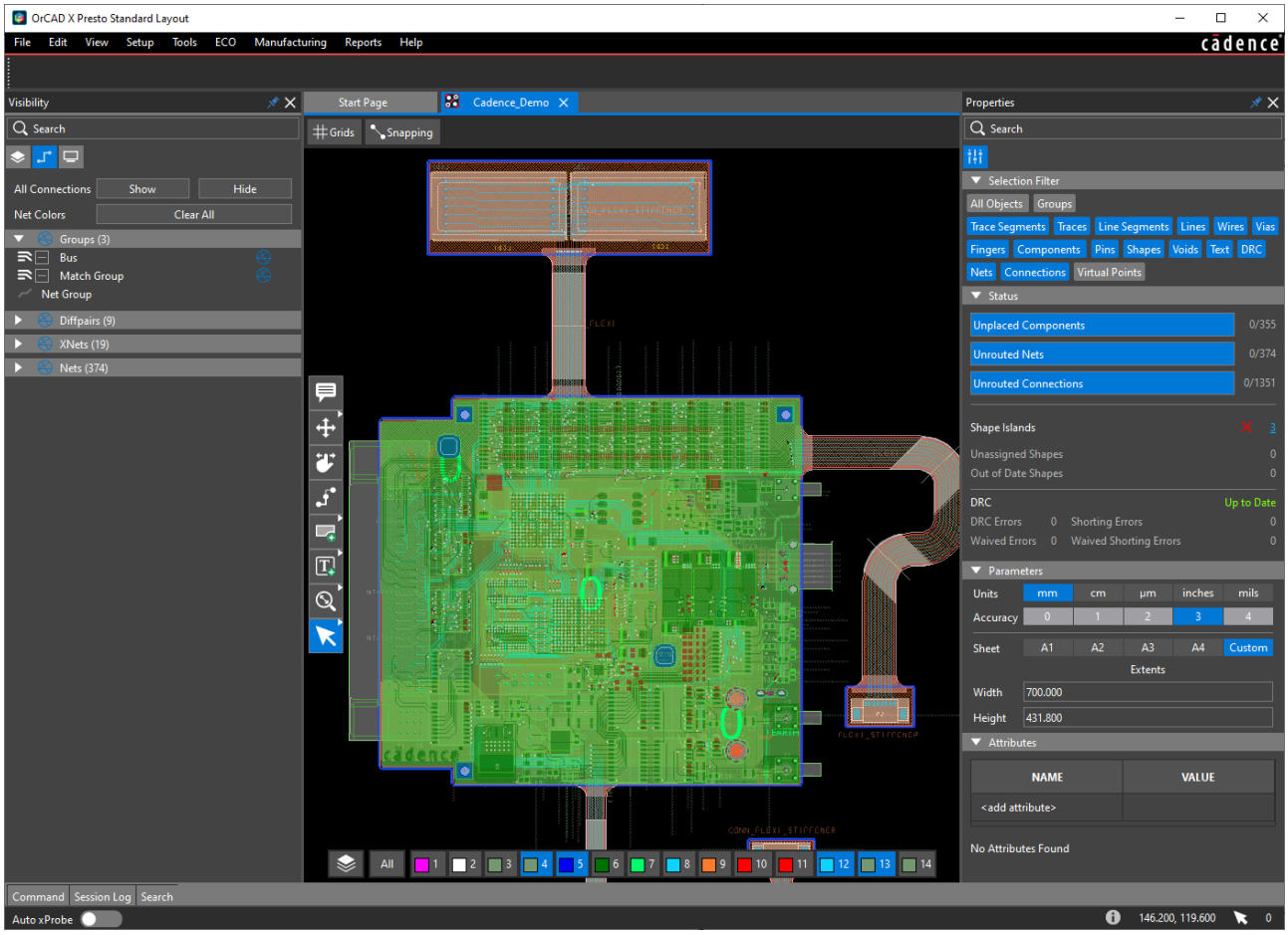
Release Changes

This section describes the release-level changes and updates in the OrCAD® X and Allegro® X products in release 23.1.

OrCAD X and OrCAD X Presto

OrCAD® X is an innovative design platform that caters to the needs of individuals and small to midsize businesses. It focuses on providing a cohesive and comprehensive solution for all design requirements. The addition of the X in this new product platform signifies its ability to extend its capabilities to the Cloud, enabling users to leverage additional services like X AI.

OrCAD® X Presto, a new layout environment within the OrCAD X platform, offers a cutting-edge solution for layout design. The interoperability between OrCAD X Presto and the existing PCB Editor ensures compatibility and easy transition of layout designs. OrCAD X Presto can be used in Cloud-connected and unconnected modes, allowing you to work flexibly based on your preferences and requirements.



The user interface of OrCAD X Presto is designed to be intuitive, capable, efficient, and accessible. It offers compact menus and a streamlined workflow, enabling you to create layout designs quickly and efficiently. The advanced features and functionalities are readily available

to deliver high-quality designs efficiently. The informative and interactive panels provide valuable insights, accelerate search and navigation, and effectively manage properties and visibility, ensuring a productive and seamless user experience.

OrCAD X Presto elevates the user experience by eliminating the need for modal dialog boxes. Instead, layout toolbars and floating menus are implemented, reducing distractions and ensuring the design space is always unblocked and accessible. This architecture significantly enhances productivity and allows designers to focus on their work.

OrCAD X Presto includes an integrated 3D viewer that seamlessly switches between 2D and 3D views. This feature enables designers to perform fast and accurate 3D analysis, supporting 3D clearance Design Rule Checks (DRCs). This integration enhances visualization capabilities, allowing the designers to identify and address potential manufacturing issues quickly and efficiently.

Operating Systems Support Changes

Support has been added for the following operating system in this release:

- Windows Server 2022

License Update

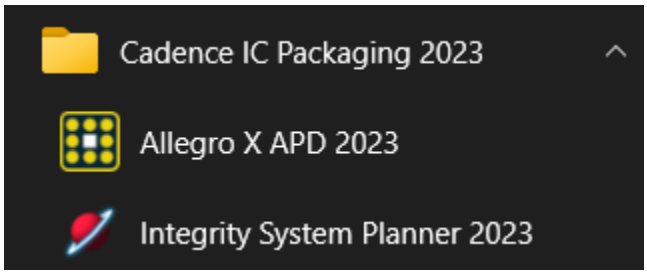
Install and configure Cadence® License Server 22.01, HotFix 002 from the Downloads page of Cadence.

Branding Updates

The Cadence IC Packaging applications have been rebranded.

- The IC package substrate layout editor is now known as Allegro® X Advanced Package Designer. Earlier, it was known as Allegro Package Designer Plus.
- The system planner and feasibility editor is now known as Integrity System Planner. Earlier, it was known as OrbitIO.

Both the products can be accessed from *Cadence IC Packaging 2023* of the Windows *Start* menu.



Software Update Notification

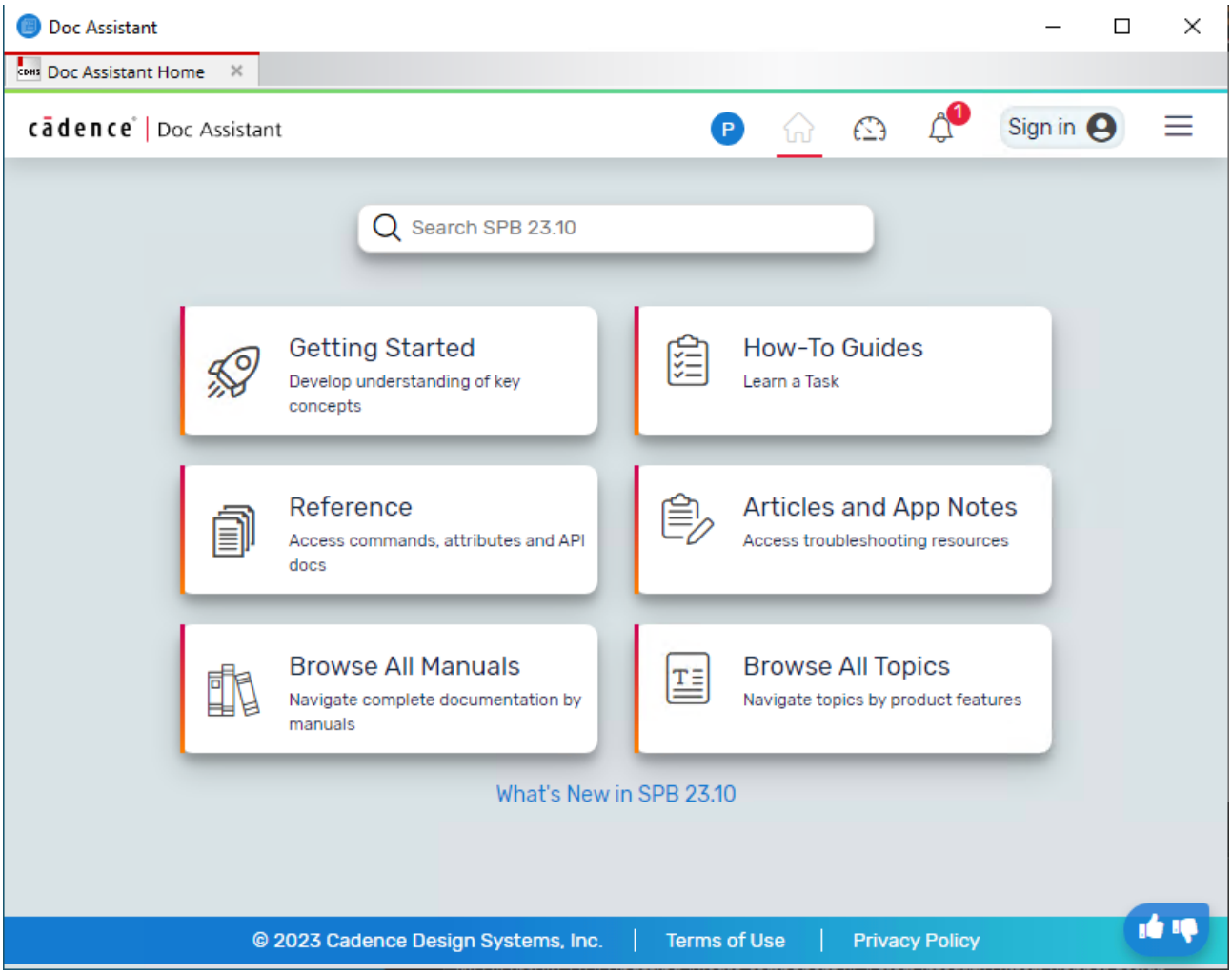
The Start Pages of applications now show a link to the latest version available for update on Windows systems. You can click the link to download and update to the latest version.

You can also choose *Help – Check For Updates* to check if updates are available.

Note: You might not be able to download or install updates if you do not have sufficient permissions.

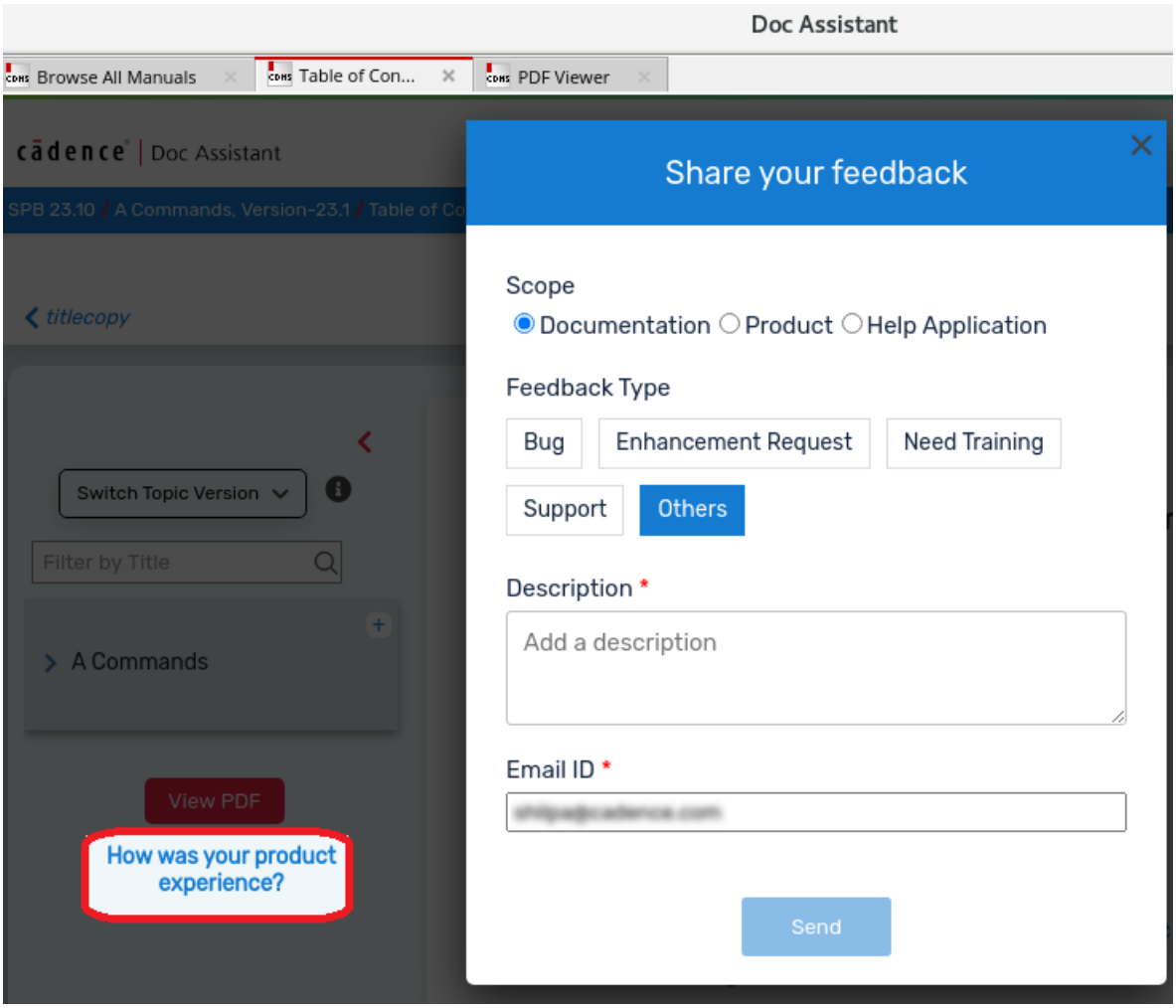
Cadence Doc Assistant

This release has a new documentation viewer, Cadence® Doc Assistant, which presents content in the form of individual, easy-to-read topics and offers a better search experience in terms of speed and relevance of results.



By default, Cadence® Doc Assistant shows you online content, ensuring that you are always accessing the latest content. However, if you are not online, Doc Assistant displays content from the installed hierarchy.

While using Doc Assistant, we encourage you to share your feedback on the content, product, and documentation viewer.



Products Not Supported on Linux

The following products are not supported on Linux in this release:

- Allegro Design Entry HDL
- Part Developer
- FPGA System Planner

Allegro X PCB Editor and Allegro X Advanced Package Designer

This section describes the new features and enhancements in Allegro® X PCB Editor and Allegro® X Advanced Package Designer in release 23.1. If a feature is available in only one of the layout editors or for a specific license, a note is provided.

Migrating Designs and Libraries to Release 23.1

You can open designs and libraries from the following releases without any migration updates and still take advantage of the latest design solutions: 17.2-2016, 17.4-2019, and 22.1.

Note: You must use release 23.1 licenses to run the release 23.1 products. However, 23.1 licenses can be used to run 16.6 or a later release.

If you save a design in release 23.1, it will be saved in the 23.1 database format and will not support compatibility with previous releases. You must run downrev (*File – Export – Downrev Design*) to be able to open the saved design in a previous release.

Library symbols and padstacks saved in release 23.1 are saved to the lowest possible database version to maintain compatibility with earlier releases with the following exceptions:

- Libraries with padstacks using Secondary Side Countersink or Counterbore or Drilled Hole values can only be used in the 23.1 release.
- Symbols with Hierarchal Route and Via Keepout shapes defined on Outer_Layer, Inner_Signal_Layers and Inner_Plane_Layers layers can only be used in 17.4 or a later release.

By default, you can downrev to the 17.4 database format, but if a design contains Nested Zones, it can only be saved to the 22.1 HotFix 003 (QIR2) database format.

Tip

You can use `dbstat` command to determine the database version of a symbol and padstack used in a library.

Related Documentation

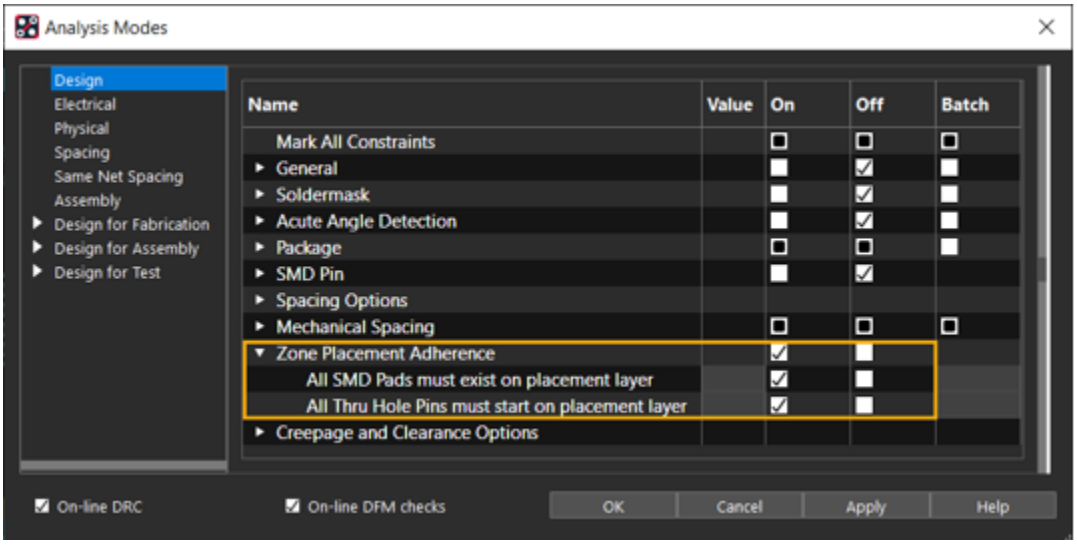
- Migration Guide for Allegro X Platform Products.

Rigid-Flex Enhancements

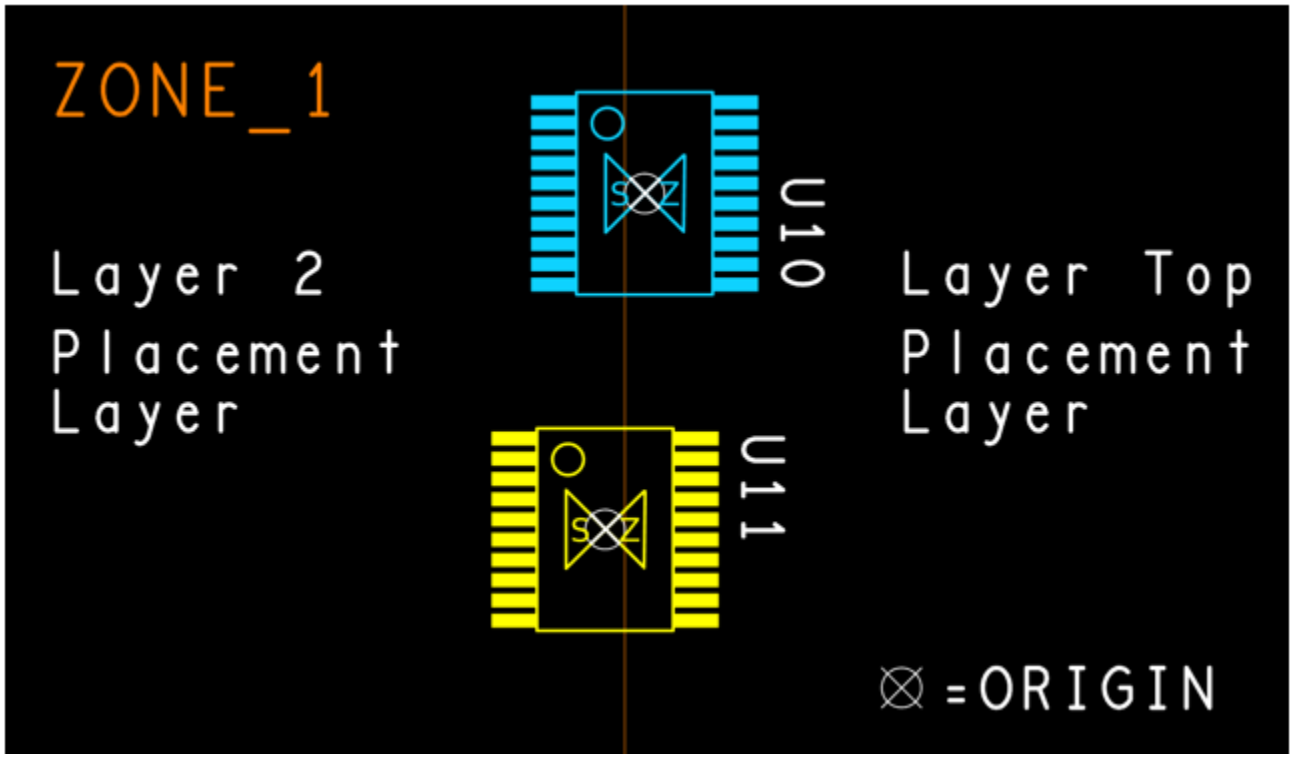
This release has the following Rigid-Flex enhancements:

Zone Adherence for Symbol Pins

There are two new Analysis Mode checks (*Analysis Modes – Design – Zone Placement Adherence*) to verify that all pin pads of a component are on the same placement layer.



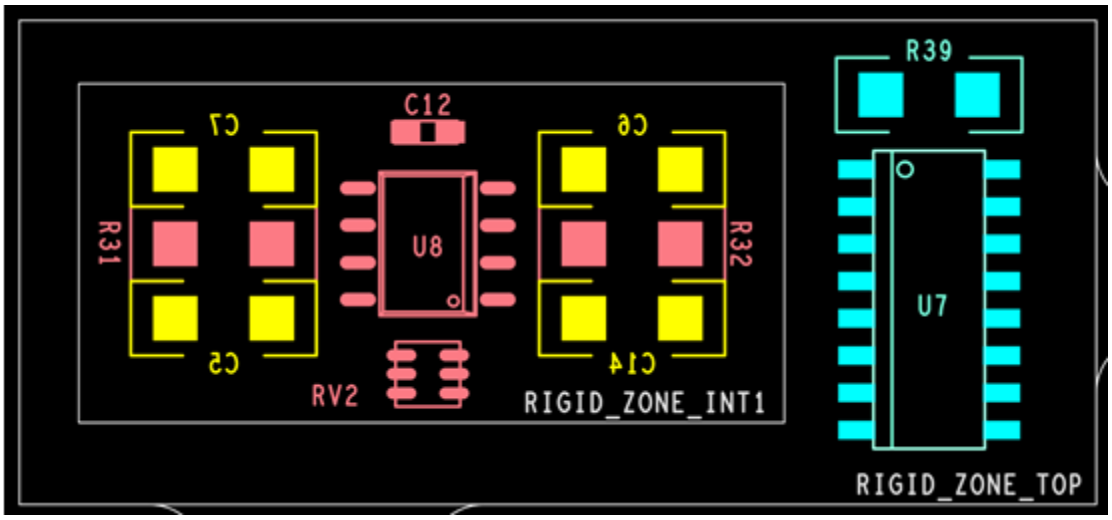
A DRC is generated if part of a pad crosses over an area where a placement layer does not exist. Components can span different stack-up areas if placement layer exists in both stack-ups, meaning that the placement layer exists in adjacent zones or zone adjacent to primary.



Nested Zones Support

It is sometimes necessary to have an area in a zone with special mask, plating, or stack-up requirements different than the rest of the zone. In these cases, a separate stack-up will be specified to drive the fabrication process to produce correct design results.

Introduced in release 22.1, HotFix 003 (QIR2), you can now have one zone surrounded by another zone, avoiding a shape creation process that is complex and error prone.



ZONE = RIGID_ZONE_TOP	ZONE = RIGID_ZONE_INT1
PASTEMASK_TOP	
SOLDERMASK_TOP	PASTEMASK_INT1
TOP (Surface)	SOLDERMASK_INT1
INT_1	INT_1 (Surface)
FLEX_1	FLEX_1
FLEX_2	FLEX_2
INT_4	INT_4
BOTTOM (Surface)	BOTTOM (Surface)
SOLDERMASK_BOTTOM	SOLDERMASK_BOTTOM
PASTEMASK_BOTTOM	PASTEMASK_BOTTOM

Zone Boundary Updates

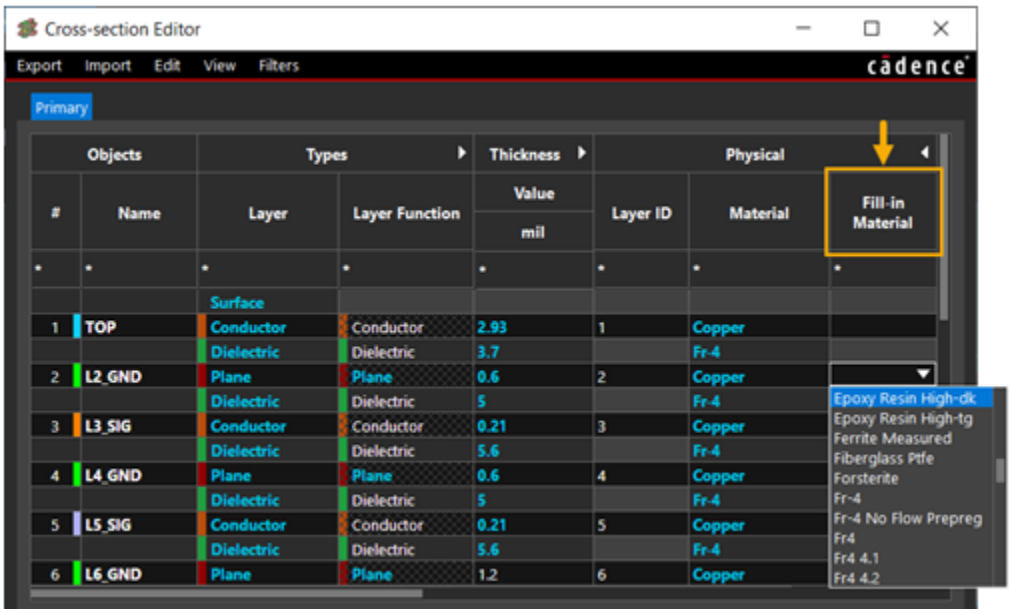
Now, you can use standard shape commands on zones, and edit zone shapes even outside the Shape Edit application mode. In previous releases, zone shape modifications were limited to the Shape Edit application mode by setting the *Enable zone boundary editing* option.

Fill-In Material (Dielectric Layers)

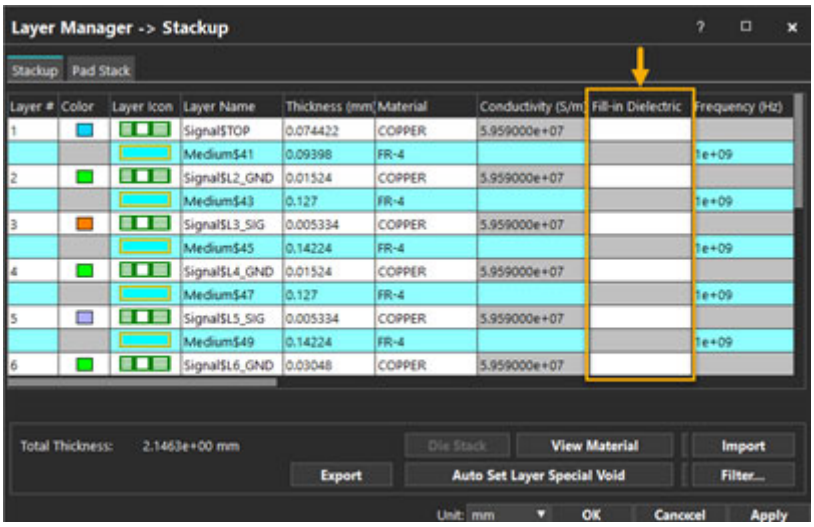
The new column *Fill-In Material* in Cross Section Editor is sourced from the common materials file (`.cmx`). The column is available on Conductor/Plane rows and is read-only for Dielectric or Named Dielectric rows.

The Fill-In Material value is supported with export or import of IPC-2581 and Cross Section files. Material defined in this column is read by Sigrity™ products for a more realistic simulation result.

The following image shows the *Fill In Material* column in Cross-section Editor:



The following image shows the equivalent *Fill in Dielectric* field in Layout Manager of the Sigrity product:

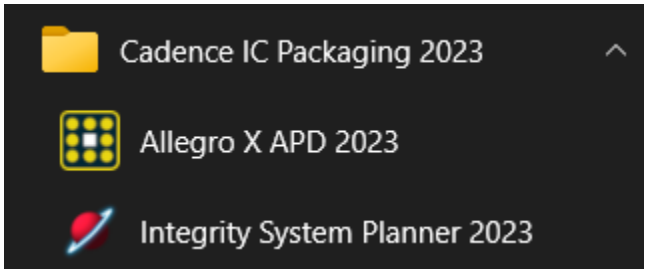


Note: Fill-In Material is deleted on downrev.

Branding Updates: Allegro X Advanced Package Designer

The constraint-driven, correct-by-design package substrate layout editor is now known as Allegro® X Advanced Package Designer.

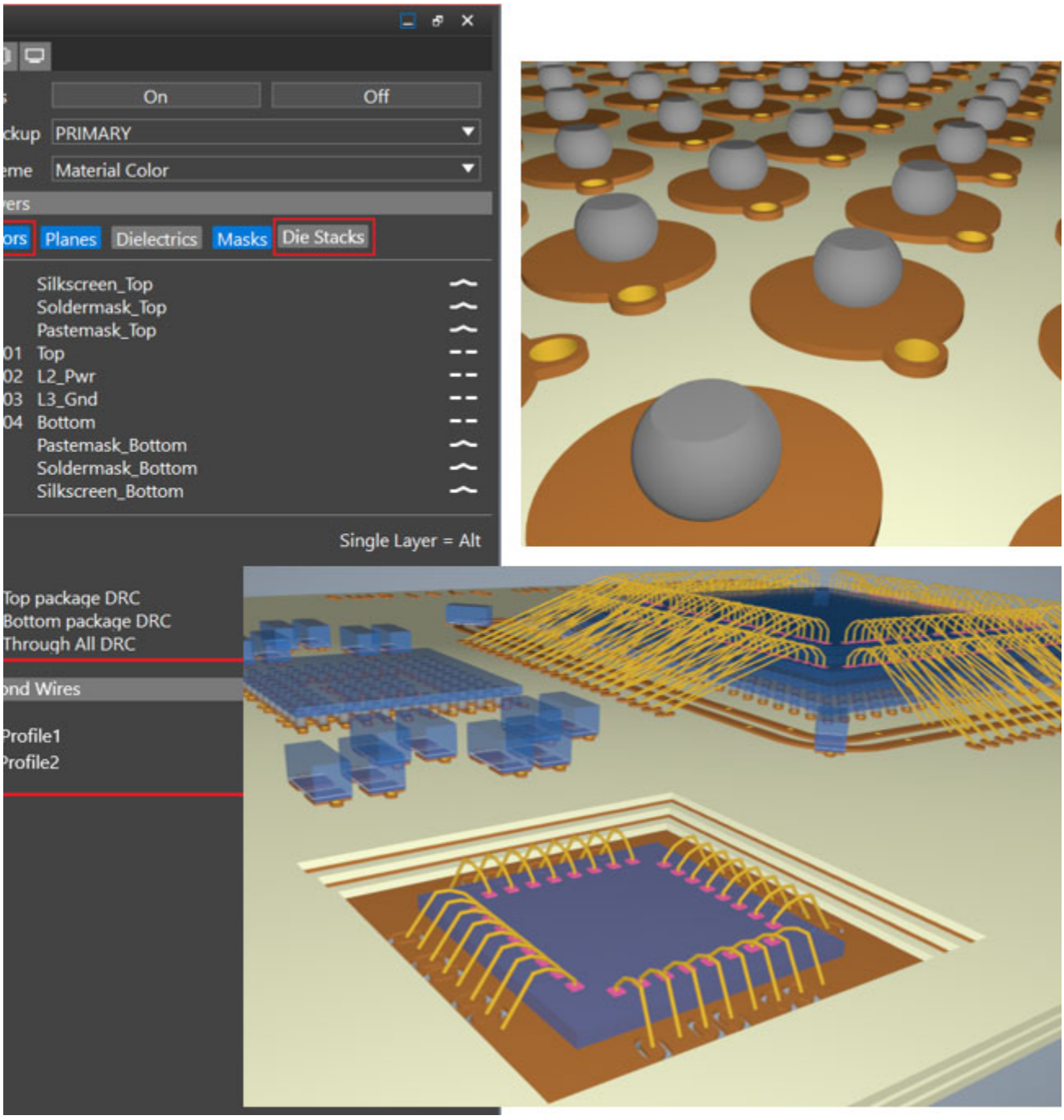
You can access the editor from *Cadence IC Packaging 2023* of the Windows *Start* menu.



Packaging Support in 3DX Canvas

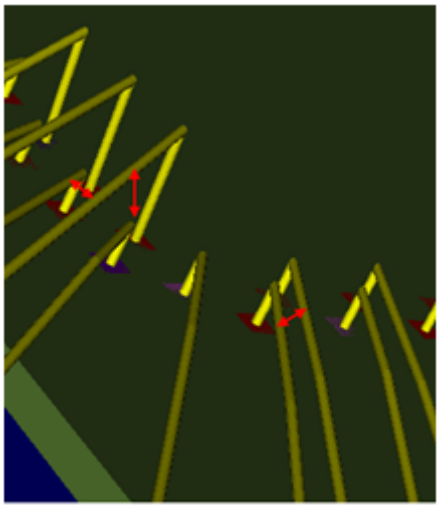
3DX Canvas addresses the scale and complexity in large modern package designs. 3DX Canvas provides highly efficient visualization representation and implementation and the new architecture enables high-performance 3D incremental updates by utilizing GPU for fast rendering.

In addition to real-time 3D incremental updates and providing 3D view in sync with all changes to database, now there is support for 3D visualization for packaging objects such as wire bonds, ball, die bump/pillar geometries, die stacks, etch back, plating bar.



3DX Wire DRCs

Constraint Manager now has 3D DRCs that are computed and checked in 3D providing real 3D checks.



You can view DRC Violations in the 2D canvas or the new 3DX Canvas.

The following DRC checks are available:

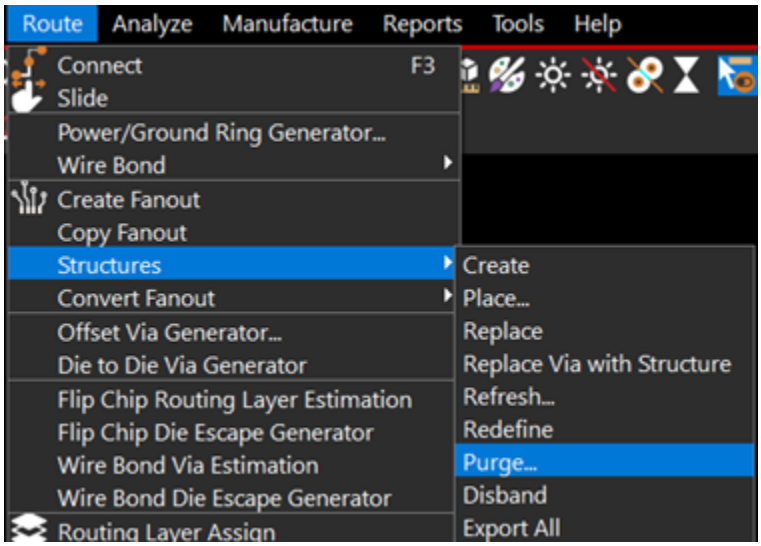
- Wire to Wire
- Wire to Finger
- Wire to Shape
- Wire to Cline
- Wire to Component

Structure Enhancements

Structures have been enhanced with the following changes:

- Purging of Structures

  You can now Purge structures to remove their definitions from the design.

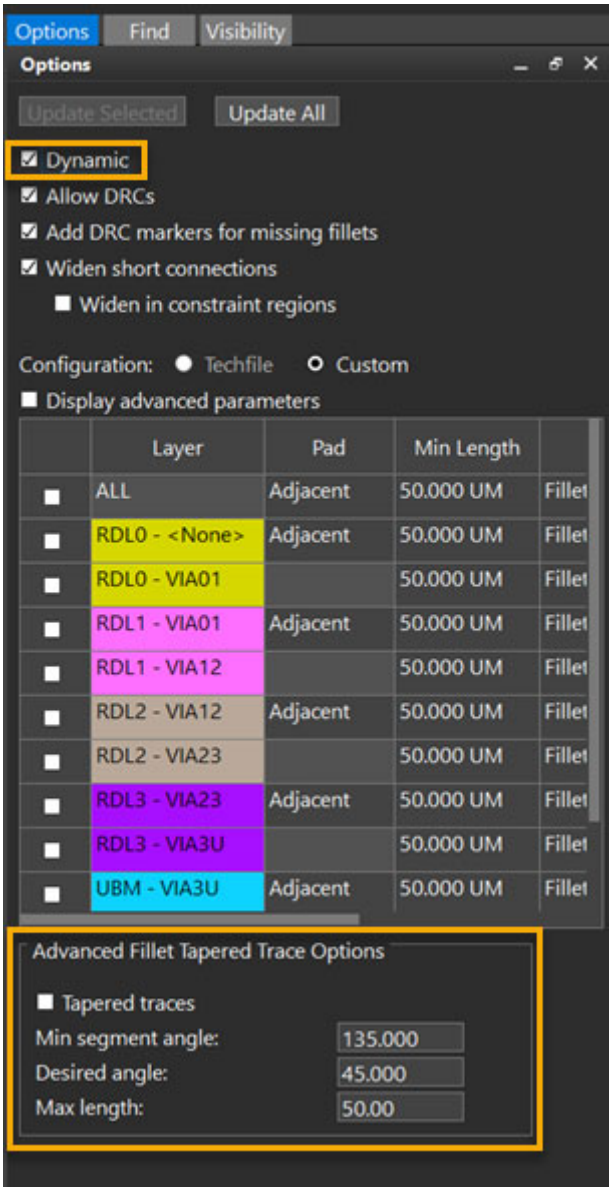


- Via Structures Loaded from Library: If you reference Via structures in subdrawing/clip files and the structures do not exist in the target design, the structures are now loaded from the library, like for other symbols.

Dynamic Advanced Fillets

Note: This enhancement is available in Allegro X Advanced Package Designer with the *Silicon Layout*.

Now, fillets are dynamically updated while routing to meet silicon fillet rules. You can also dynamically add tapered trace fillets as you route using Advanced Fillets.

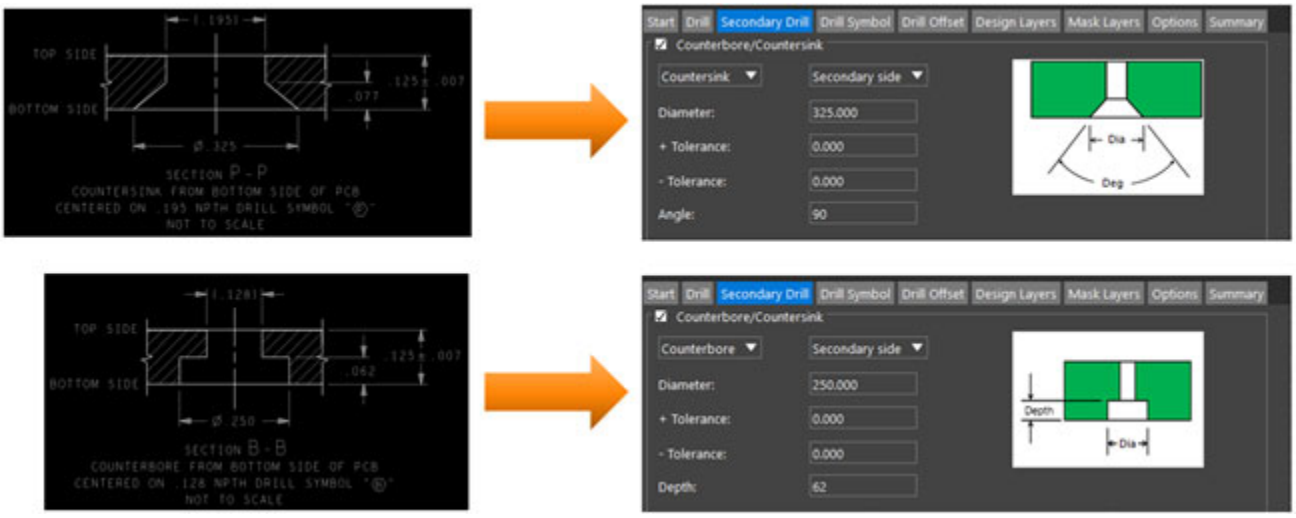


Padstack Editor Enhancements

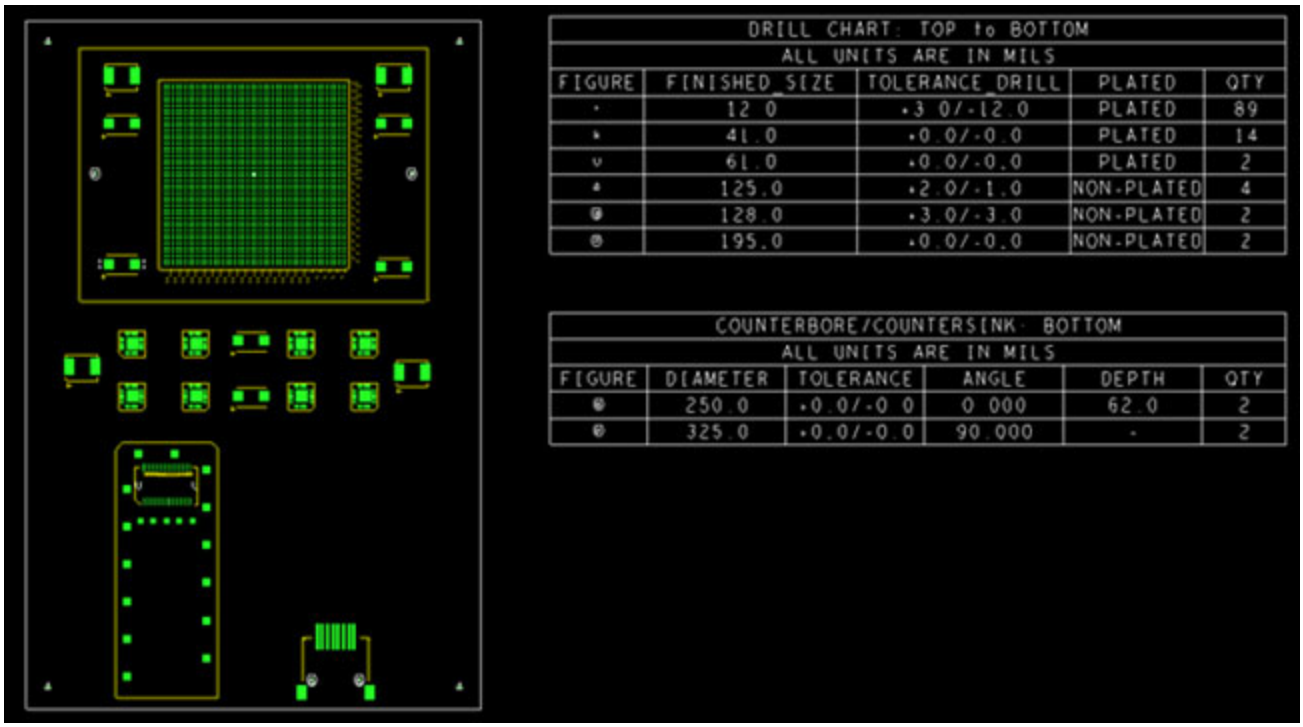
Following are the enhancements available in Padstack Editor in this release:

Counterbore and Countersink Secondary Side Definition and Reporting

Now, you can define counterbore or countersink from either the primary or the secondary side, and are not bound to the side the component is placed on.



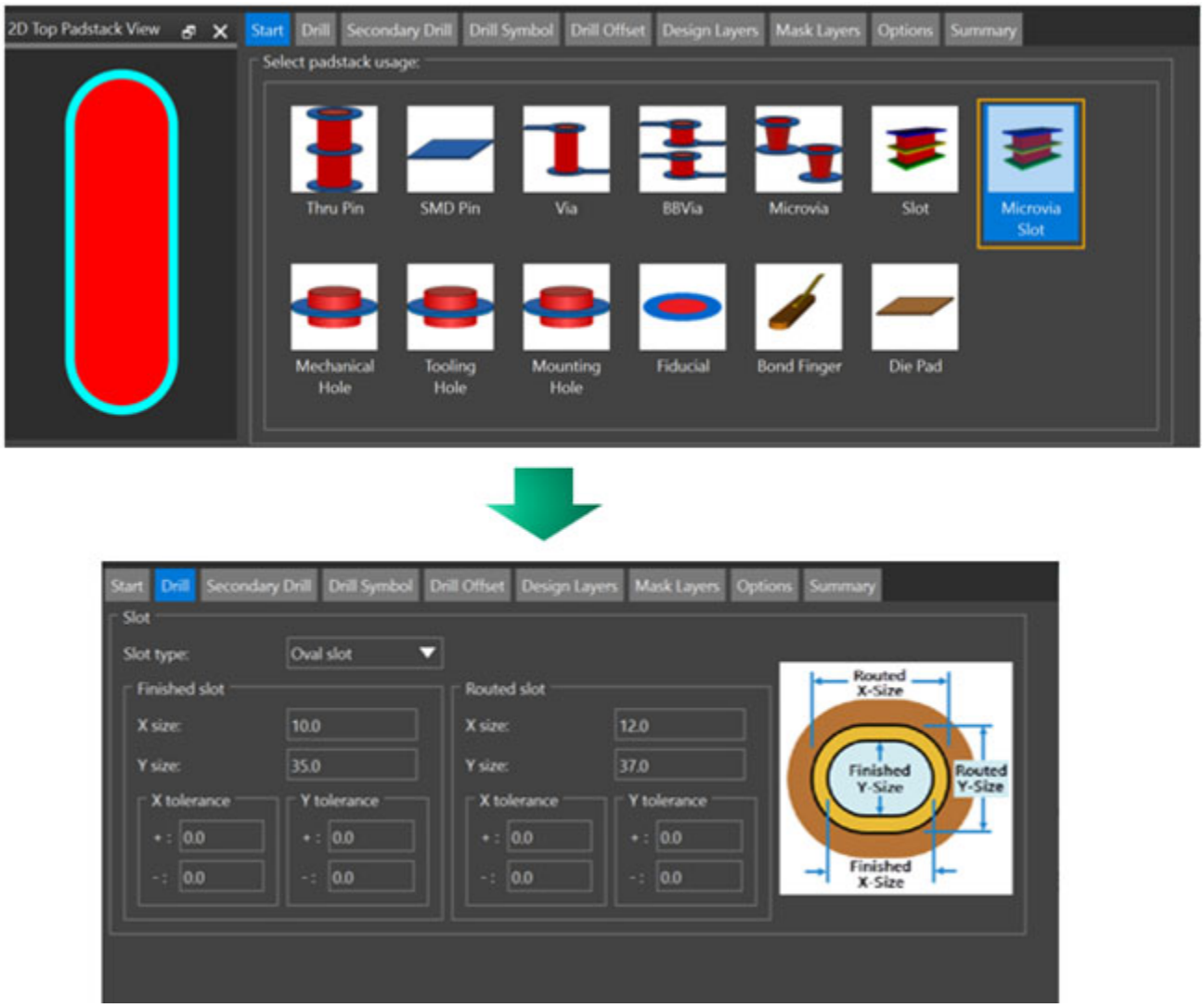
You also do not need to inform the fabricator about secondary drill requirements separately because Drill Legend and NCDrill Export now report when drilling is required from secondary side.



Note: If you need to downrev a release 23.1 design, you must manually remove any counterbore or countersink that exist in the secondary side.

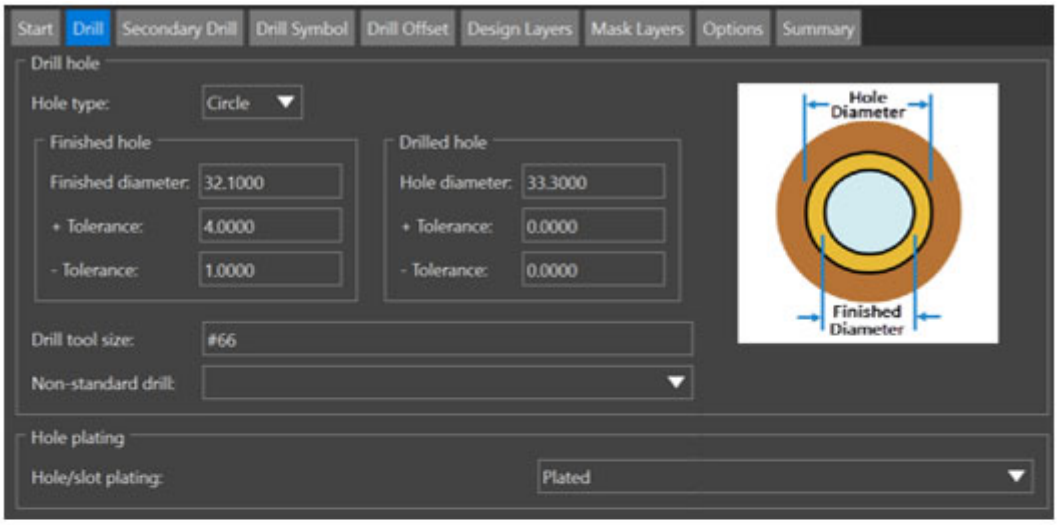
Oval and Rectangular Slots for Microvia Padstacks

You can now use oval and rectangular slots in microvia padstacks These slots are in addition to the existing circle and square plated holes. The new slot types follow the standard Microvia constraints.



Drilled Holes/Slots Before Plating

You can now specify accurate size for drill holes or routed slots before the holes are plated to ensure the holes or slots are not damaged during assembly, for example, for Press Fit connectors.

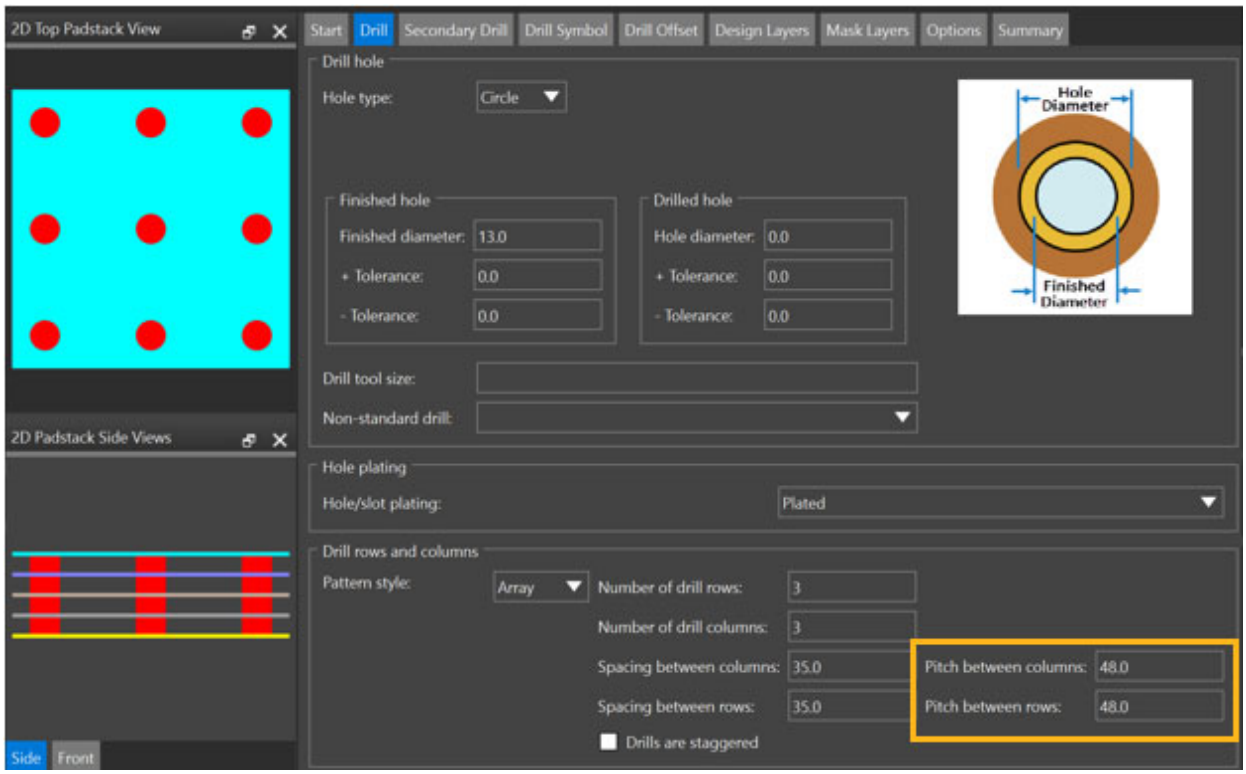


You can specify circle or square holes for Drilled Holes and rectangle or oval slots for Slot Holes. You can also specify a tolerances for the hole or slot size.

Note: During downrev, any drilled holes will be removed from the padstacks of the design.

Calculated Spacing for Multi-Drill

Now, you can specify pitch values for the rows and columns for a multi-drill and the spacing is automatically calculated.

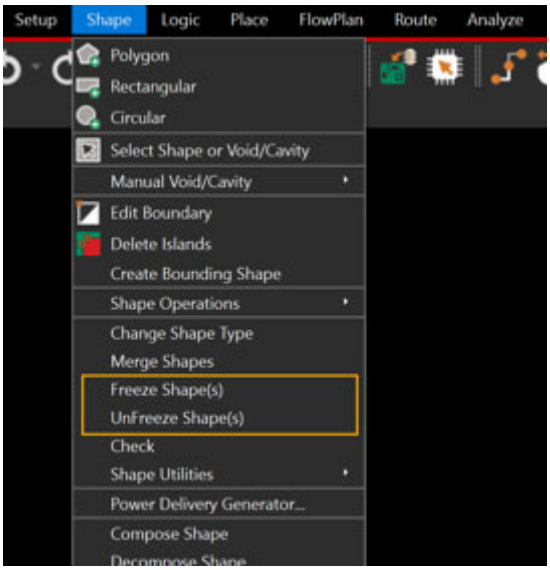


Dynamic Shape Update: Frozen Shapes

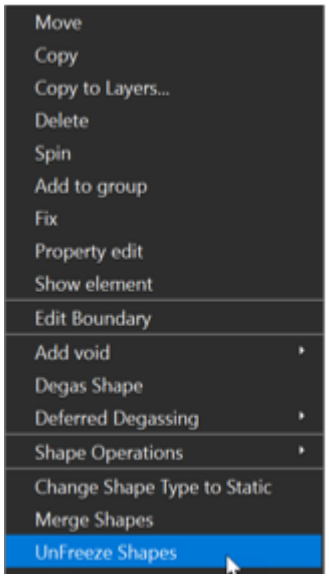
Dynamic shapes are automatically updated when interacting with other objects, but you can now freeze the shapes without changing them to static; for example, to maintain design intent by protecting critical circuitry drawn using shapes.

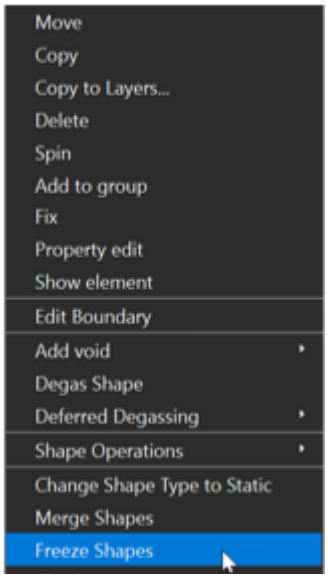
Once a dynamic shape is frozen, new objects entering the dynamic shape area will not void and generate a DRC error like with a static shape. You can manually modify shape boundaries on frozen dynamic shapes to maintain current voiding while avoiding new voids.

Choose the *Freeze Shape(s)* or *Unfreeze Shape(s)* command options from the *Shape* menu to freeze or unfreeze a dynamic shape.

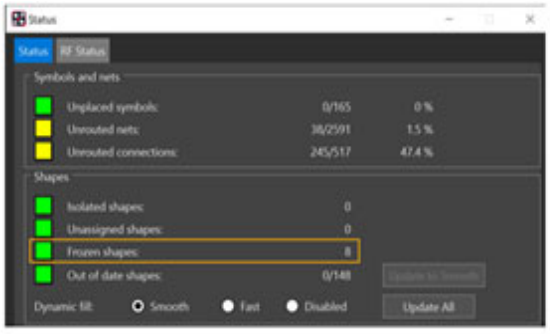


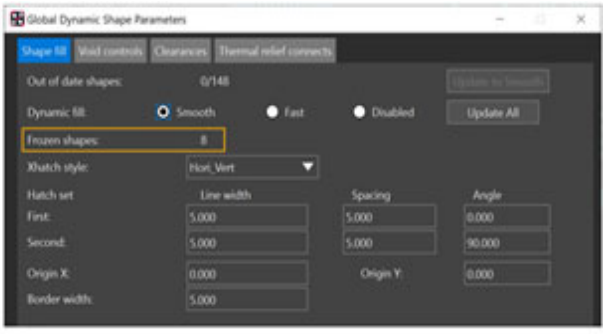
You can also select a shape and then choose command from the context menu.





All reports, such as Design Status, Shape Parameters, Shape Reports, Show Element, or Find By Query, that show Dynamic shape status also show frozen shapes.

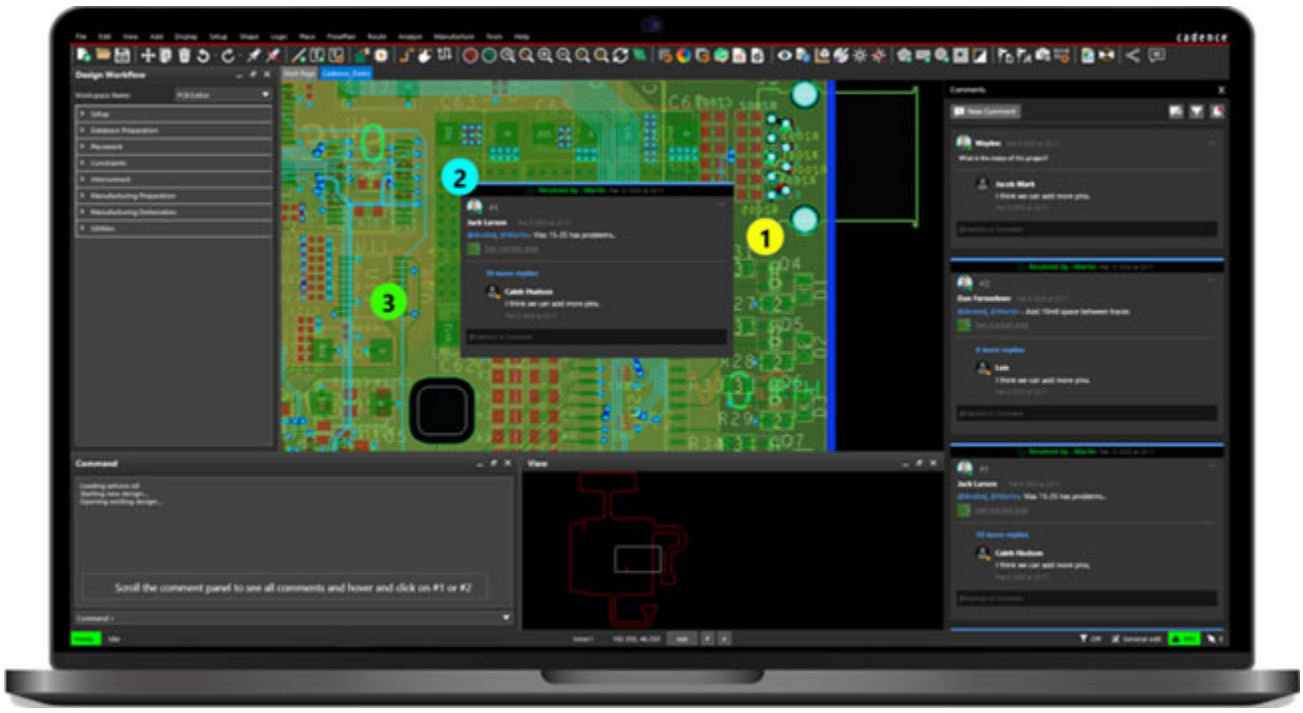




Design Review and Markup

This release has the new Design Review and Markup feature enabling the review and tracking of designs through markups. The markups are stored in the database with tracking comments. You can recall a markup with canvas auto-centering and layer display.

Note: This feature is available in Allegro®, Allegro® X, OrCAD® X licenses and Allegro® X System Capture licenses that allow the edit of layout databases.



Usability Enhancements

This release has the following usability enhancements:

Allegro X - 3D Canvas Update

It is now easier to map 3D Models and output 3D representation.

3D Model Mapper in Symbol Editor

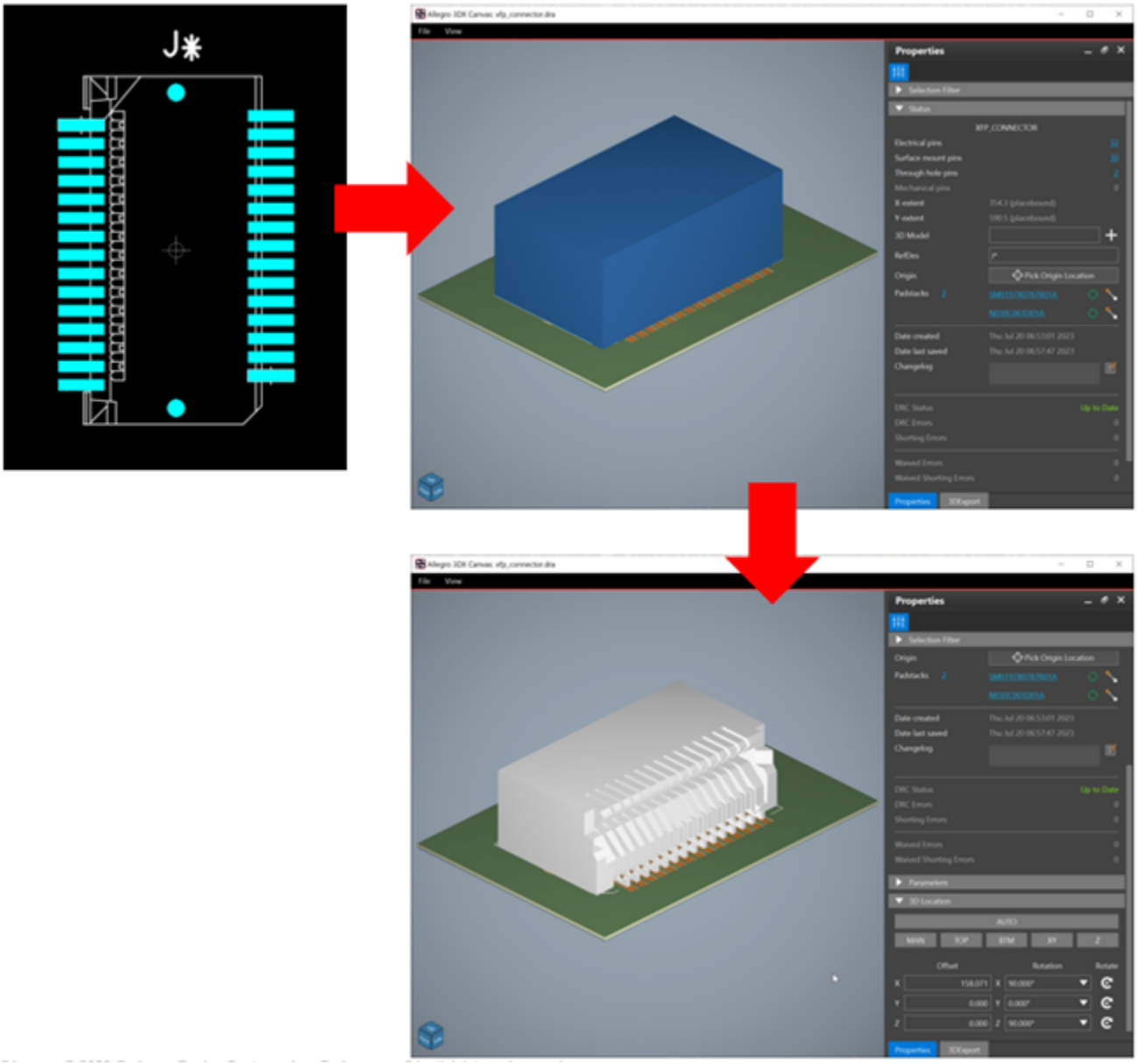
You can now map 3D Models to footprints directly in the library without the need for STEP models on the disk.

To assign a model to a footprint and view in the layout, do the following:

1. In the *Properties* tab, select the STEP model.

2. Under *3D Location*, click *AUTO* and then fine tune the X-Y-Z placement.

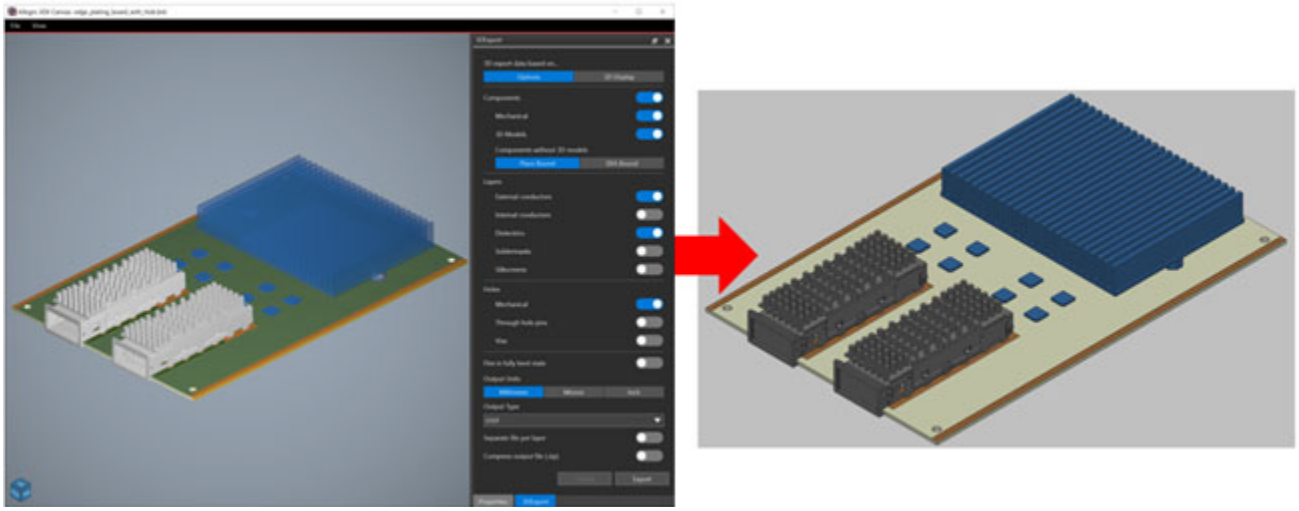
   Footprint Model assignment is visible in the layout.



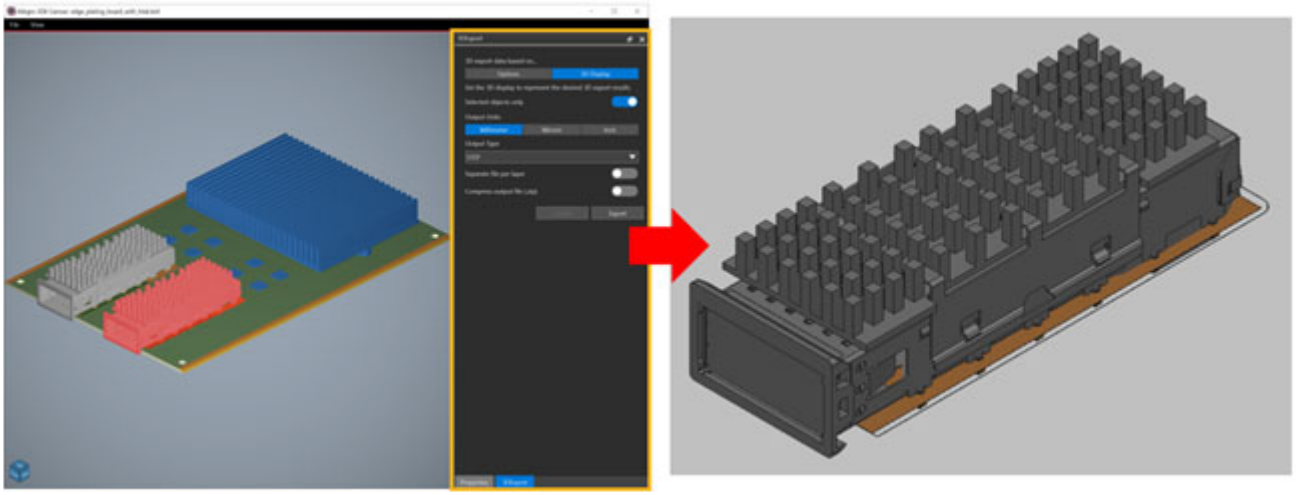
3D Model Export Support

You can now output complete 3D representation of the entire design or 3D representation of based on visibility settings.

To output a complete 3D representation, select the required output from the 3D Export tab and then click *Export*. You can select from any one of STEP, IGES, ACIS, or PDF.

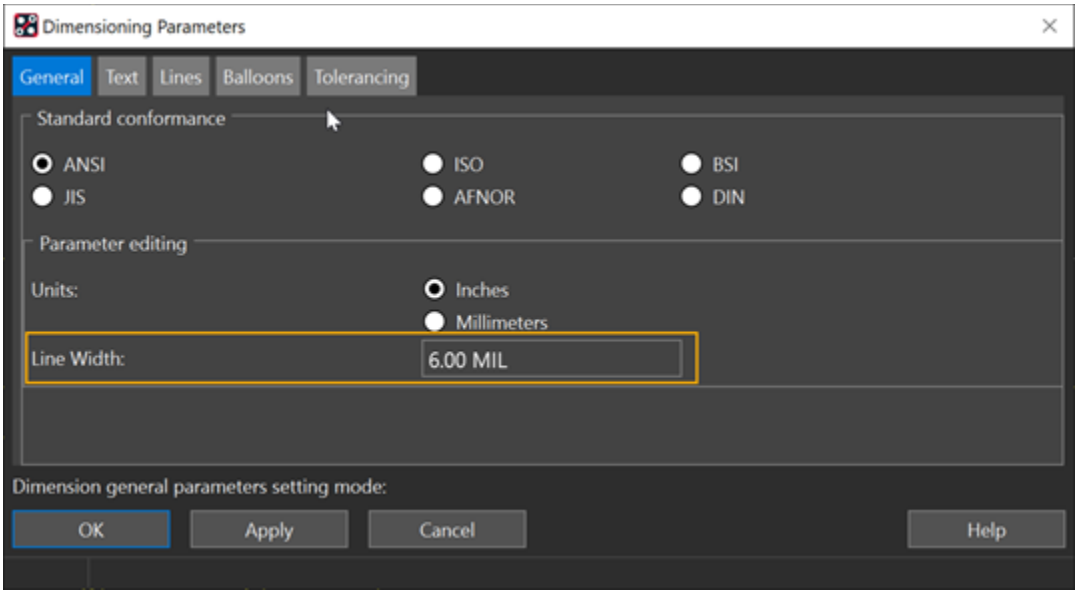


To output 3D representation based on visibility settings, set Selected objects only.



Dimension Environment Update

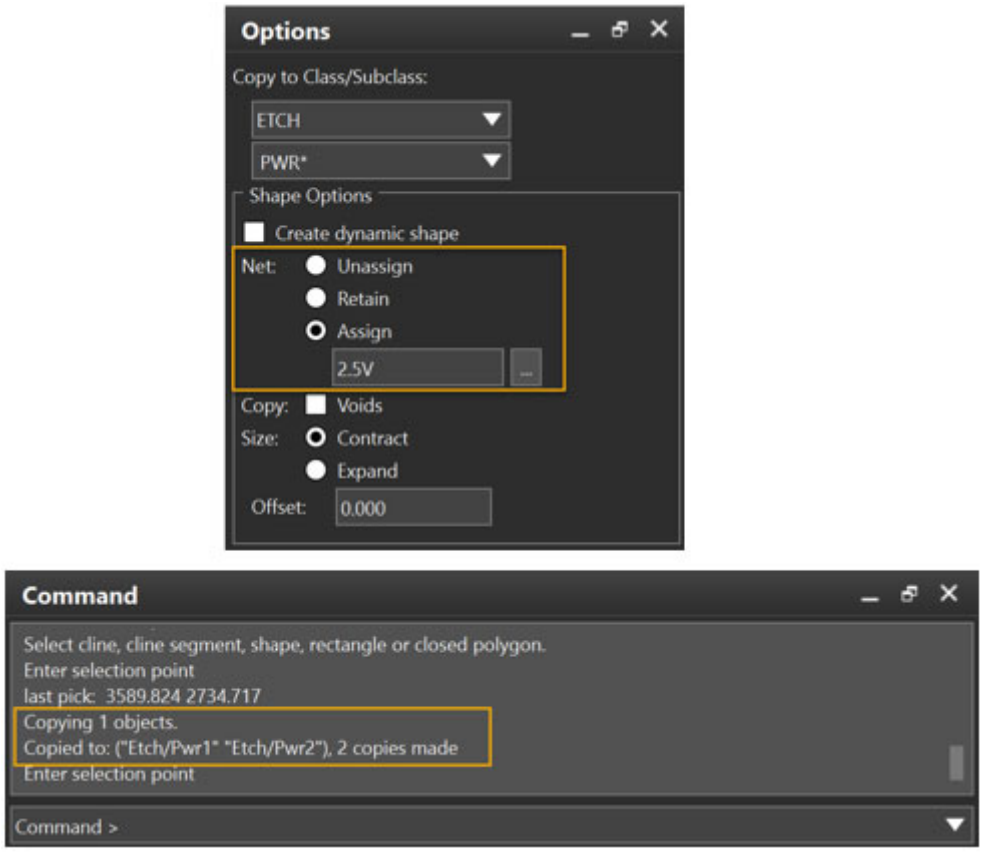
Use the new *Line Width* parameter to apply a line width to dimension lines.



Without the line width, the dimensions were drawn with thin (0-width) lines as shown in the following figure:

Z-Copy Enhancements

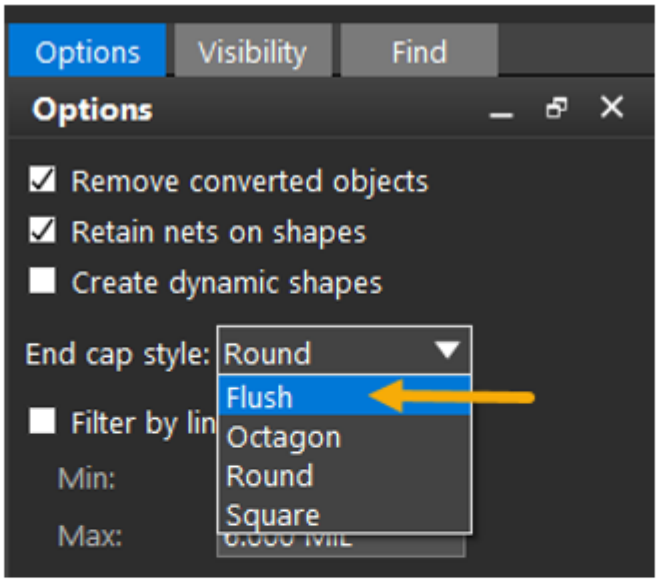
Copying etch shapes to other layers has become easier with Z-Copy using the new *Net* options that save extra steps on canvas to adjust shape Net Name on copies.

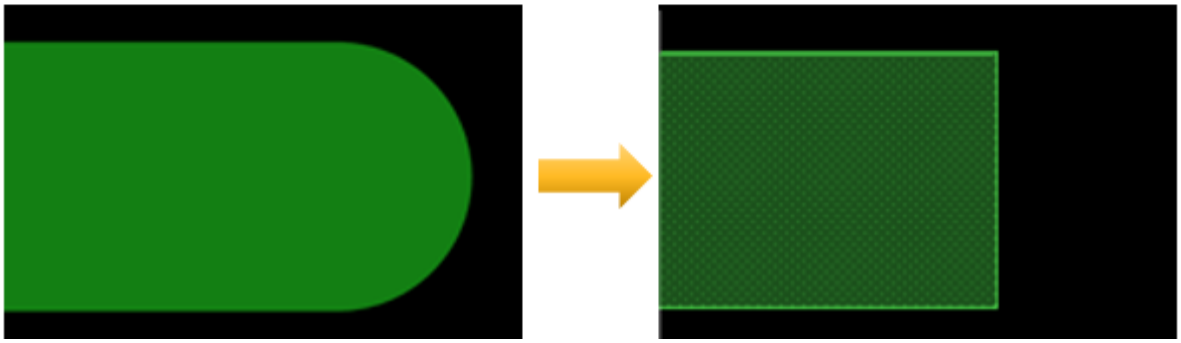


Note: You can use a wildcard in the target layer name to copy a shape to multiple layers.

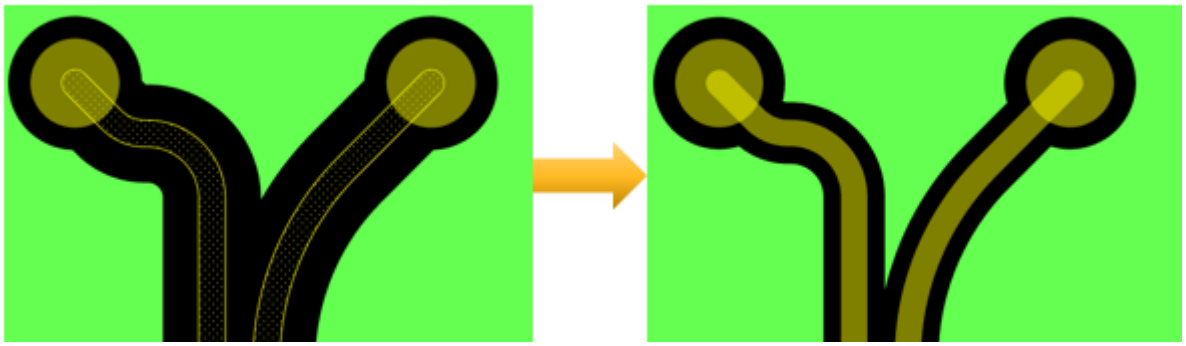
Enhancements to the Convert Cline or Line to Shape Utility

Tools – Convert contains several conversion utilities to convert between object types. The Cline / Line to Shape utility has been enhanced to include an additional *End Cap Style* called *Flush*.





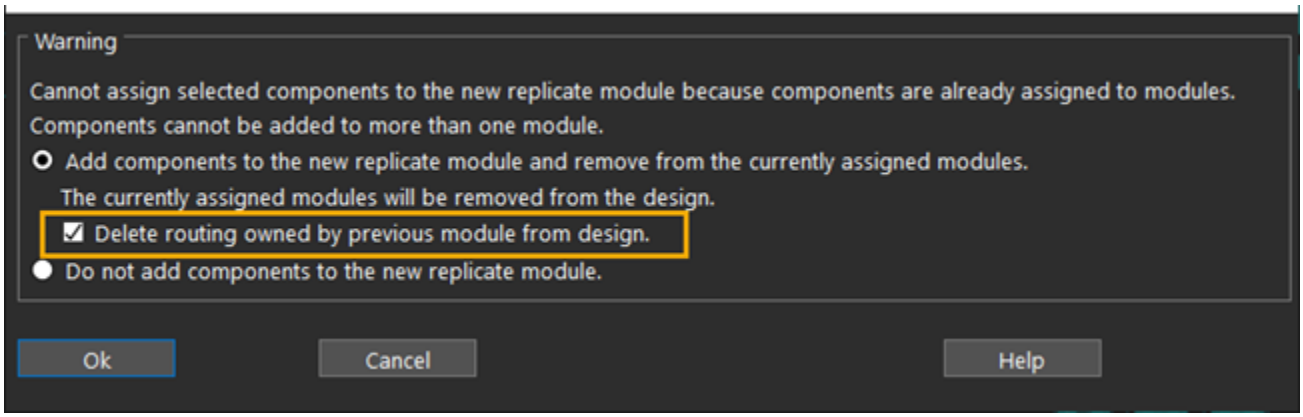
In addition, converting Shapes with arc segments now converts to Clines Arcs.



Place Replicate Apply Enhancements

Components can only be a member of one Place Replicate module at any given time. It is possible to re-apply a component or group of components to a new replicate module, but it leaves behind any connected copper features from the previously applied module. You must manually remove routing that is left behind.

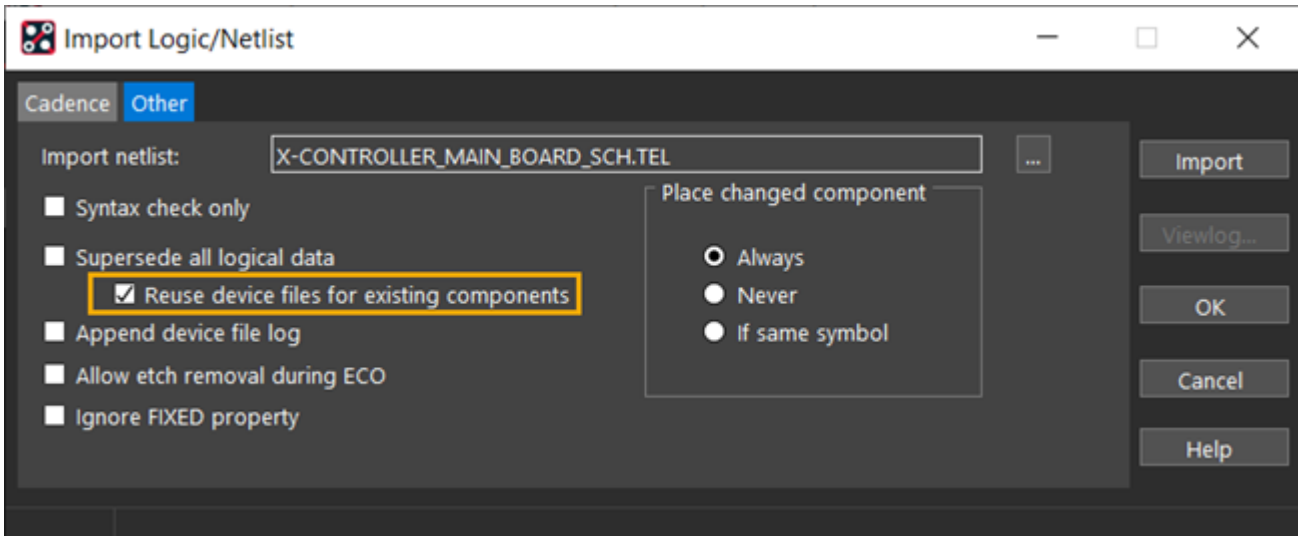
You can use the new option *Delete routing owned by previous module from design* in the Warning dialog box to remove the routing from previously applied modules.



Third-party Netlist Import

You might be receiving a new netlist several times during the design process. Devices files are required to import a netlist successfully.

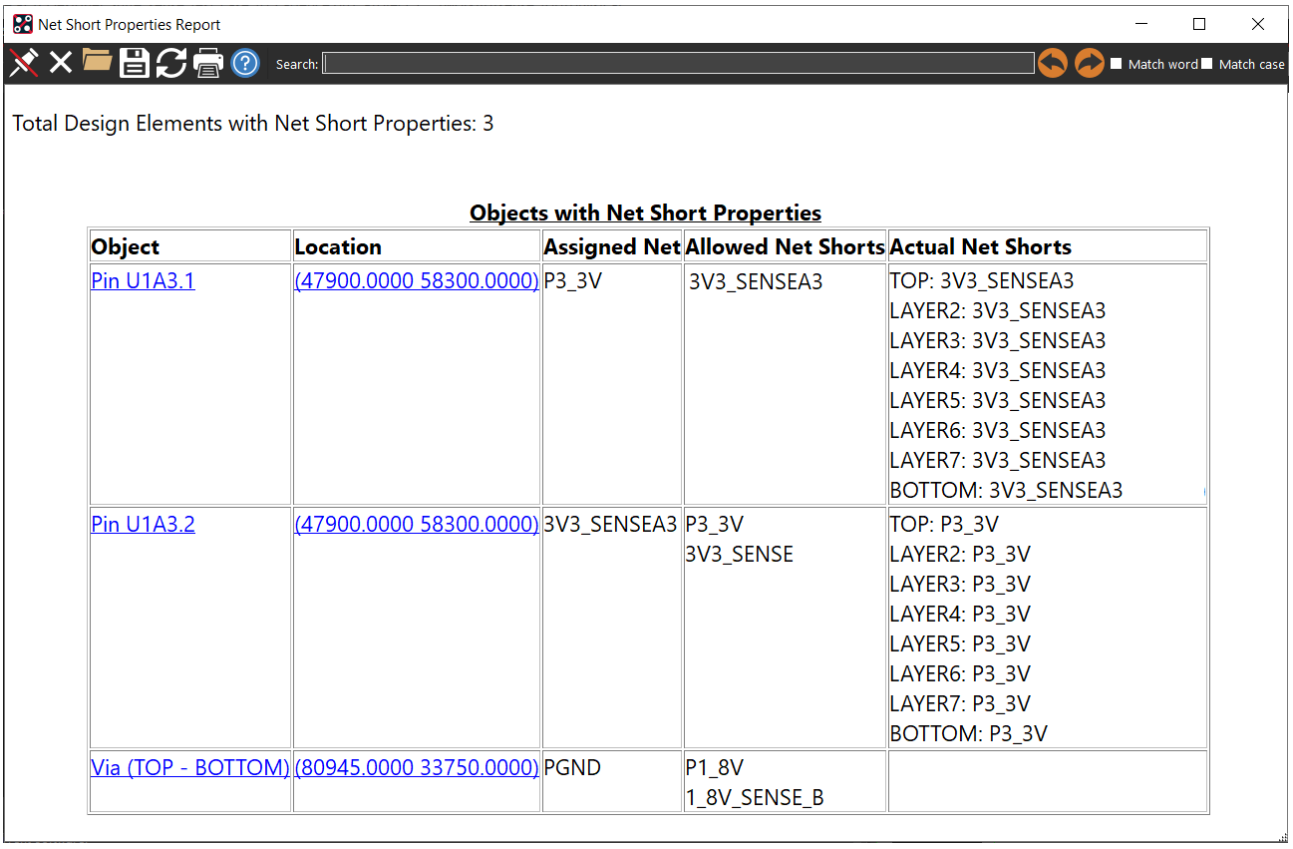
A new option *Reuse device files for existing components* has been added to reuse Devices Files that are currently in a design, eliminating the need to export them out of the design every time a netlist import is required.



Net Short Report

You can create a direct short in a design by adding a NET_SHORT property to the objects and then shorting Net Name. You must then verify manually that all the required shorts have been made.

You can now use the new Net Short Properties report to verify shorts. This report lists all objects in the design with NET_SHORT properties along with the layers that the short occurs.

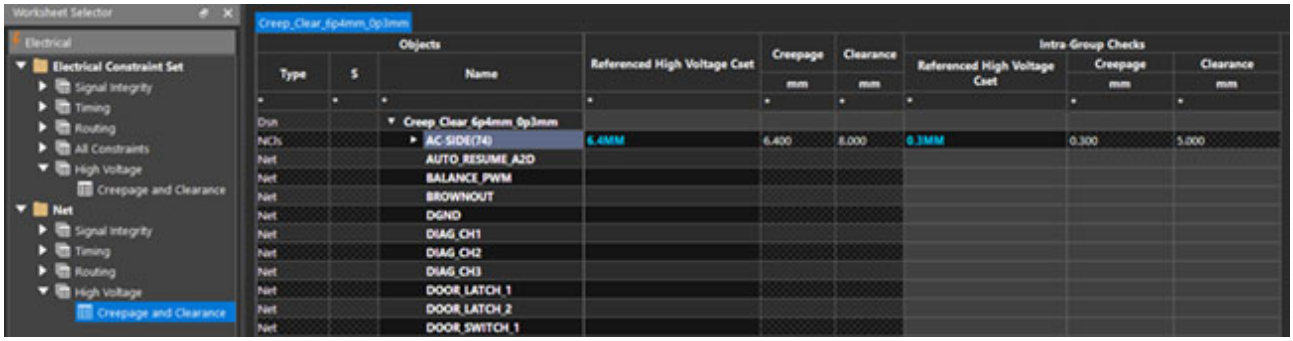


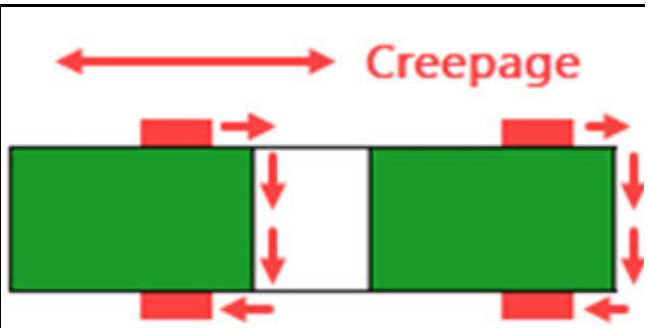
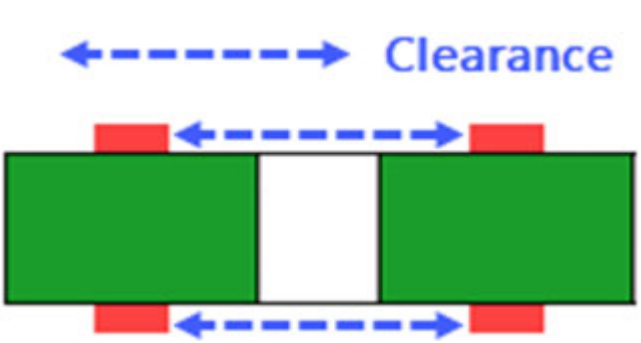
Object	Location	Assigned Net	Allowed Net Shorts	Actual Net Shorts
Pin U1A3.1	(47900.0000 58300.0000)	P3_3V	3V3_SENSEA3	TOP: 3V3_SENSEA3 LAYER2: 3V3_SENSEA3 LAYER3: 3V3_SENSEA3 LAYER4: 3V3_SENSEA3 LAYER5: 3V3_SENSEA3 LAYER6: 3V3_SENSEA3 LAYER7: 3V3_SENSEA3 BOTTOM: 3V3_SENSEA3
Pin U1A3.2	(47900.0000 58300.0000)	3V3_SENSEA3	P3_3V 3V3_SENSE	TOP: P3_3V LAYER2: P3_3V LAYER3: P3_3V LAYER4: P3_3V LAYER5: P3_3V LAYER6: P3_3V LAYER7: P3_3V BOTTOM: P3_3V
Via (TOP - BOTTOM)	(80945.0000 33750.0000)	PGND	P1_8V 1_8V_SENSE_B	

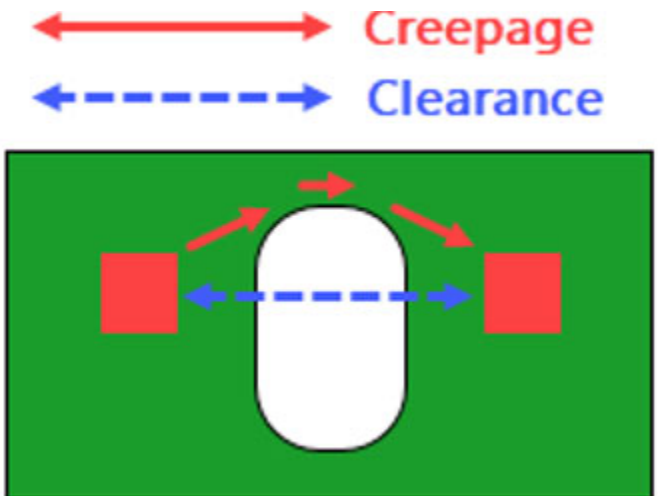
Creepage and Clearance Checking

Note: This feature is available only for Allegro X Venture and Enterprise licenses.

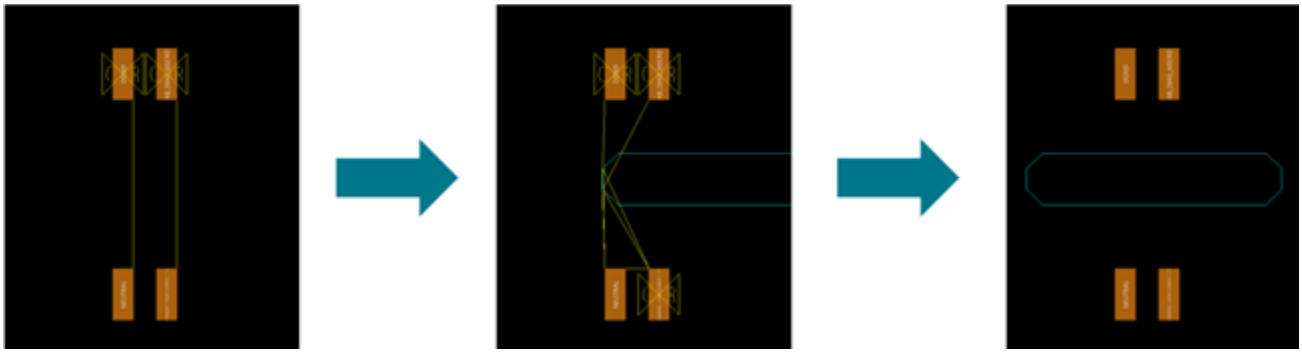
You can use the new High Voltage Constraint checks to verify creepage and clearance rules.



Creepage: Distance measurement along surface of material between high-voltage objects.	
Clearance: Spacing measurement through the air between high-voltage objects.	

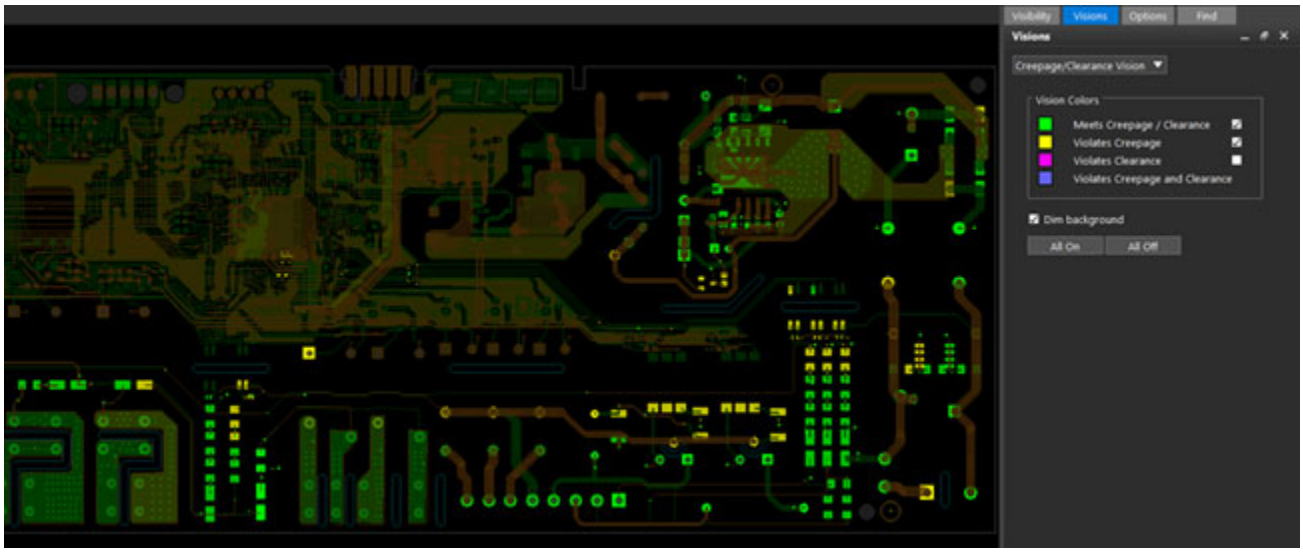


The DRC system recognizes non-plated slots added between two high-voltage objects to increase creepage, and recalculates the creepage around the slot while clearance is measured across the slot opening through the air. Creepage measurement jumps across slot openings when distance is less than Pollution Degree defined in Analysis Modes (*Setup – Constraints – Modes - Design Settings*).



Note: Design Outline notches and Multi-Layer stack-up might not calculate Creepage distances correctly. This will be addressed in a future HotFix.

You can use the Creepage/Clearance Vision to review the DRC errors. The Vision provides graphical feedback with color coding directly on canvas.



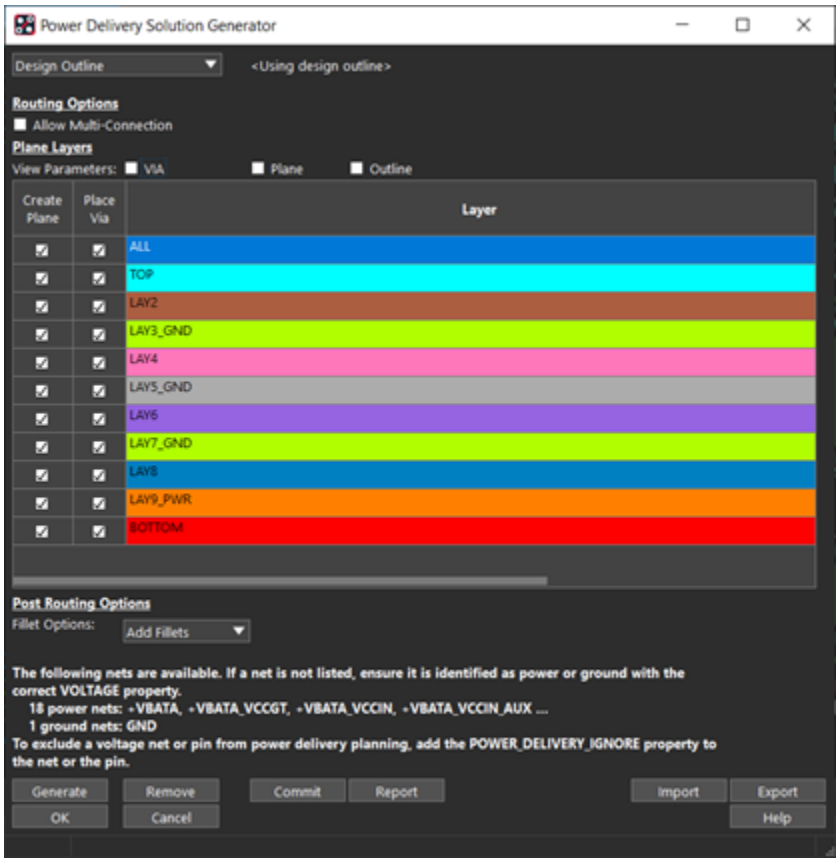
Power Delivery Generator Enhancements

Note: This feature is available in *Allegro X Advanced Package Designer* with *Silicon Layout*, *Allegro Enterprise PCB Designer*, and *Allegro X Venture Layout*.

You can use Power Plane Generator to quickly generate planes for a section of the design or the entire design based on pin placement for voltage nets. You can also review power plane escape and adjust placement or constraints to improve power connections.

Now, you can select different parameters for a basic or an advanced mode.

If you do not select any of the Via, Plane, or Outline parameters, you can generate planes in the basic mode with minimal setup for fast results with little to no learning curve.



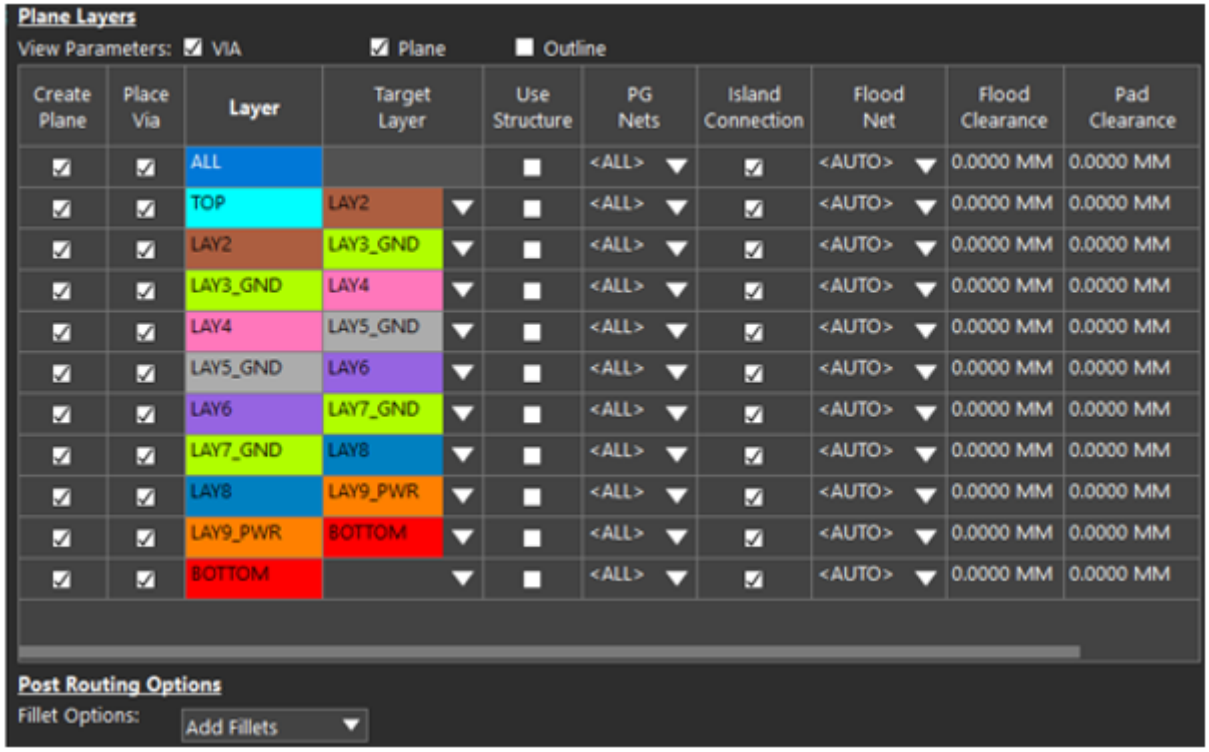
You can select to view parameters for Via, Plane, and Outline to access additional columns for a more detailed settings to control plane generation:

- Select *Via* to be able to stitch Via and Structure controls from current layer to a target layer.

- Select *Plane* to indicate specific details for Plane construction.
- Select Outline to be able to specify the shape outline controls.

Depending on the selection you see the following columns:

Column	Description	Available for Parameters
Use Structure	Select to use via structures for Power/Ground connections.	Via
PG Nets	Specify All, Ground, or Power nets (Nets with VOLTAGE property) on a per layer basis or define specific nets and priority per layer.	Via, Plane
Island Connection	Set to Allow trace connections to isolated vias.	Plane
Flood Net	Specify Flood Net (Voltage Nets) to backfill layer after plane generation.	Plane
Flood Clearance	Specify Flood Net Shapes inset for specific area outline.	Plane
Pad Clearance	Specify pad expansion to determine plane shape edge.	Plane
Plane Corners	Specify shape outline corner to be used (45° or 90°).	Outline
Plane Grid Snap	Set to snap each shape outline vertex to the etch grid.	Outline



Performance Improvements

Performance has improved substantially in features related to modules and in the 3DX Canvas application.

The module flow has up to 60X improvements in the following aspects:

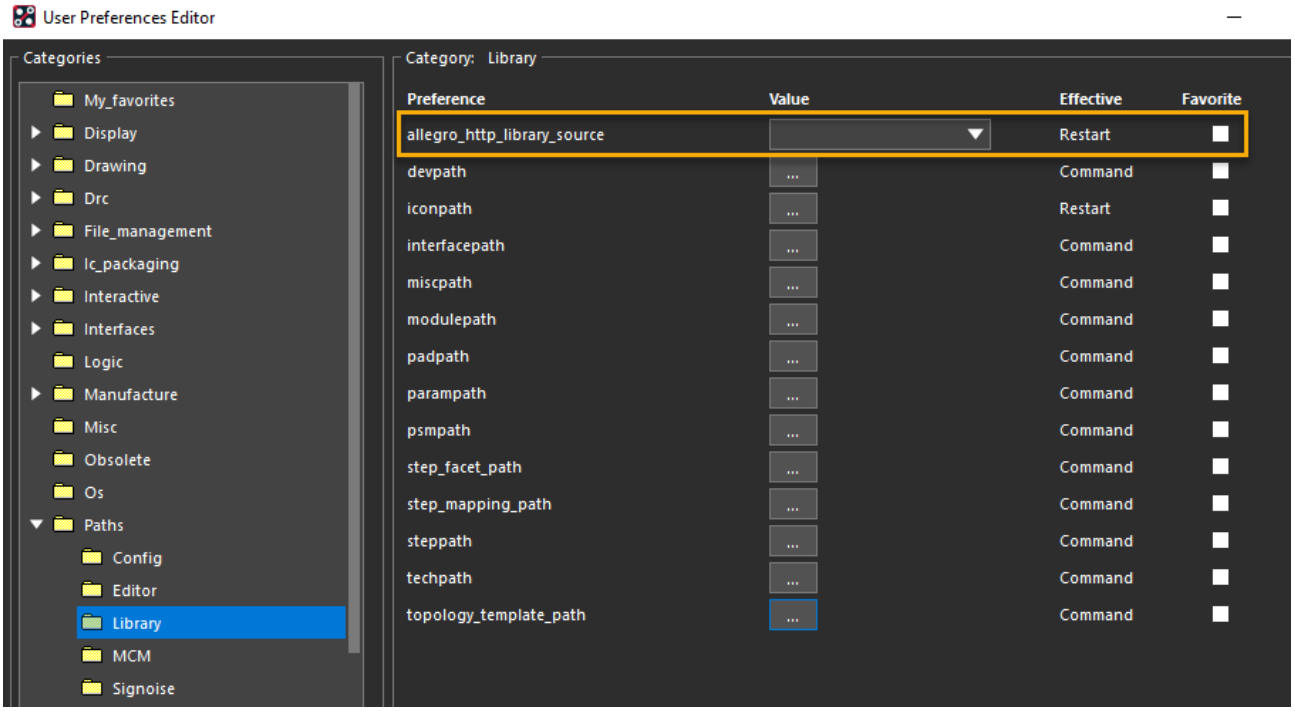
- Creation of modules
- Creation of Place Replicate modules
- Placement of modules
- Refreshing modules
- Replacement module definition
- Disbanding of modules

The 3DX Canvas has demonstrated improvement compared to the legacy 3D applications in speed and memory utilization. The loading of designs is now at least 20 times faster and there is a 10X reduction in memory usage for large designs.

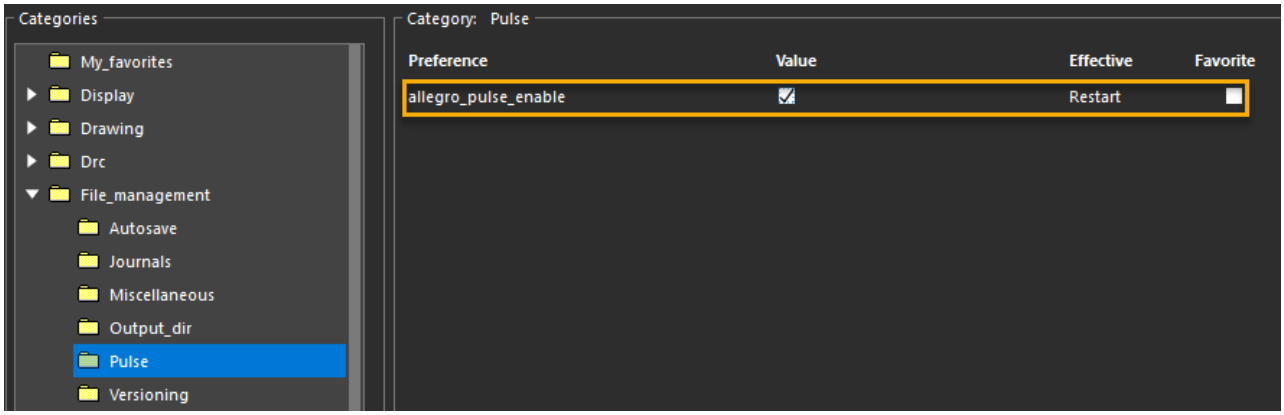
Library and Symbol Updates Using Allegro X Pulse

Note: These enhancements are only available in Allegro X PCB Editor.

You can now search and download library elements, such as padstacks or shapes, using the HTTP protocol instead of only accessing libraries on disks using the PSMPATH and PADMPATH variables. You can set *allegro_http_library_source* under *Paths – Library* to EDM to specify the source as a Pulse server or set the to OrCAD X Cloud to query and download library elements from the Cloud. You must restart the application after setting the variable to see the changes.



You can now use Symbol Revision Manager (*Place – Symbol Revision Manager*) to update Allegro symbols without the Flow Manager if you set *allegro_pulse_enable* under *File_management – Pulse* and restart the application.



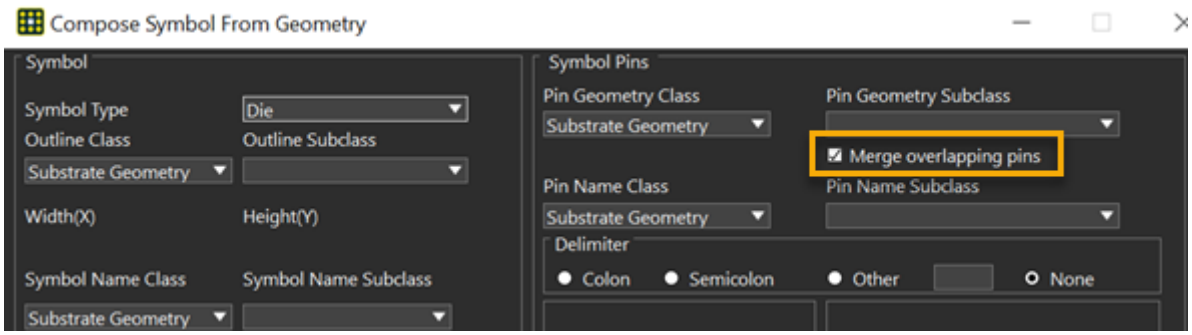
Miscellaneous Enhancements

This release has the following miscellaneous enhancements:

Compose Symbol Merge Option for Overlapping Pins

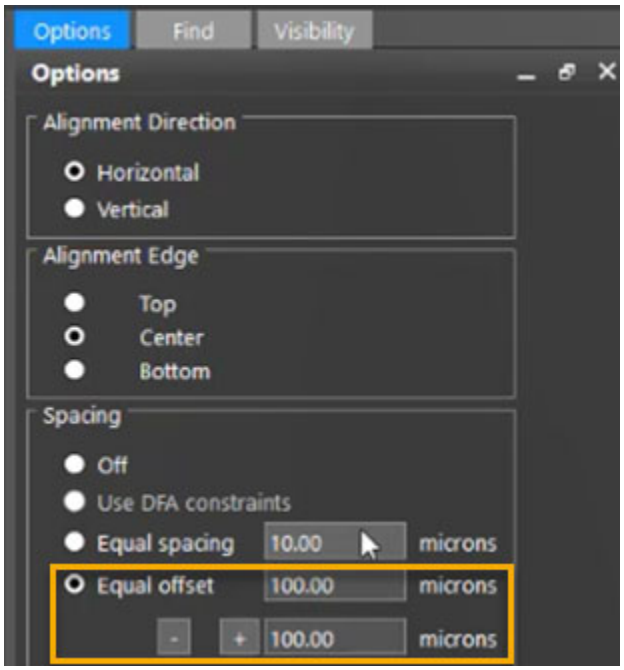
Note: This feature is available only in Allegro X Advanced Package Designer.

You can now select to merge two pins that touch or overlap into a single pin using the *Merge overlapping pins* option in Compose Symbol from Geometry. The option is selected by default.



Aligning Components by Offset

Now you can align components using the new offset mode. Selecting the new mode gives center to center offset with stepping increments.

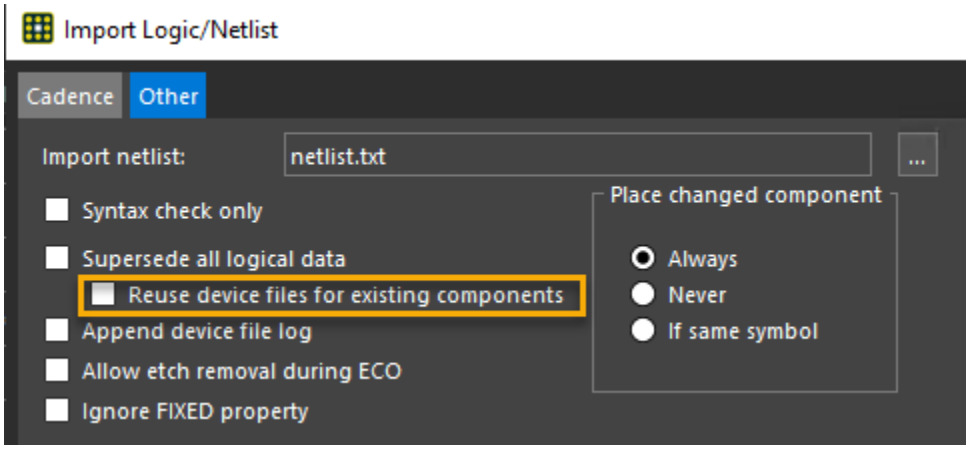


Retaining Original Definition After Optical Die Shrink

You can now save the original definition of a die in the database on applying an optical shrink.

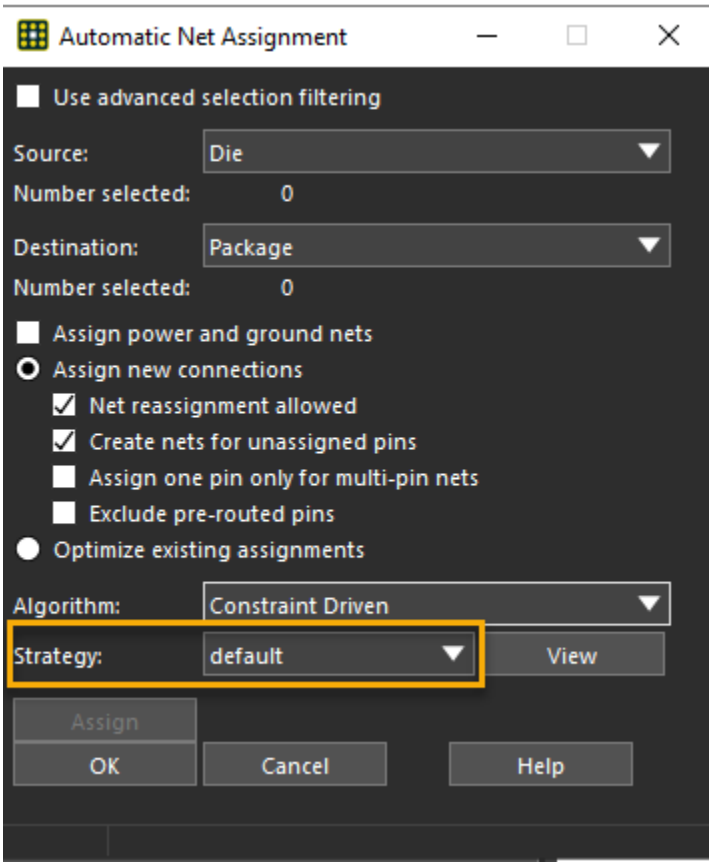
Device File Reuse for Existing Components for Netlist and Logic Import

Now, you can reuse device files for existing components without first adding the components to libraries even for net name changes. The Import Logic/Netlist dialog box (*File – Import – Logic/Netlist*) now has the *Reuse device files for existing components* option. This option is not selected by default.



Easy Access to Strategy Files

Now, you can easily access strategy files while assigning nets automatically in the constrained-driven flow.



You can have different weights for objects depending on the type of nets being assigned.

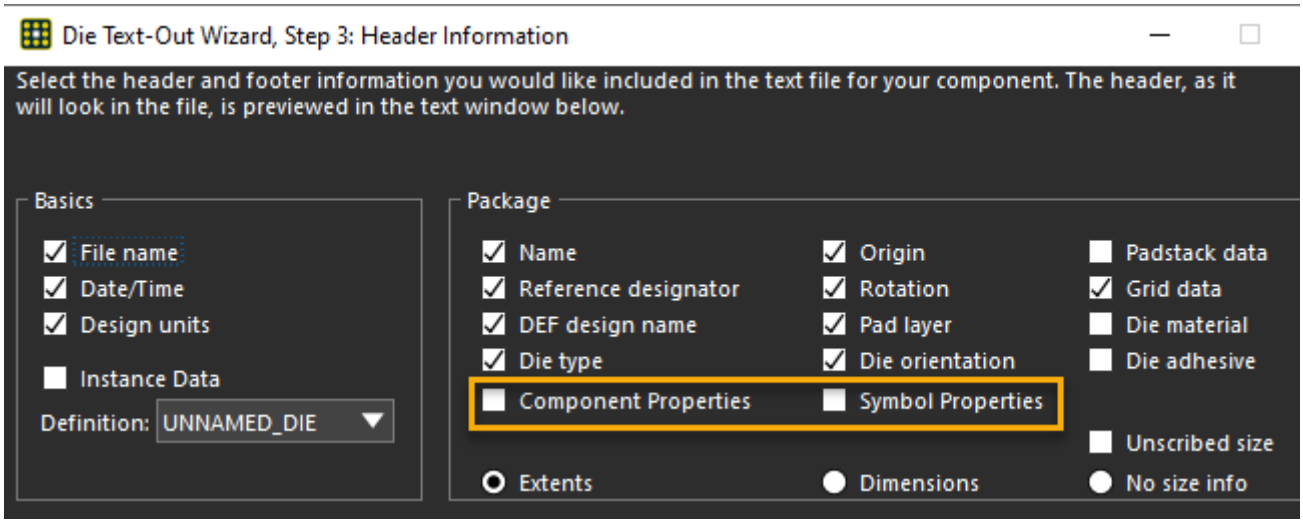
```
#########################################################
# Weighted Rules (0 = unused; 1 = min; 99 = max penalty) #
#########################################################

AssignAllNets                99
PhysicalViolation            95
DiffPair                        90
MinLength                       95
MaxLength                       95
RelativeLength               85
MatchLength                     80
PinCode                         50
SwapCode                        25

#################################
# Assignment Parametric Controls #
#################################

HowHardToTry                 Low                              # Low | Middle | High
DiffPairOrientation          Adjacent                  # Adjacent | Tandem | Diagonal
AssignFirst                         RingToRing                  # Middle | Corners | RingToRing
LayerBalance                 EvenDistribution       # FillLayers | EvenDistribution
NetLengthBalance             Average                   # Average | Minimize | Maximize
MultiNetScheduling           Independent               # Independent (pin to pin) | MST
```

Text Wizard Enhancements

Text wizards have been enhanced with the following changes in this release:

- Export and import symbol and component properties.

  Now, you have options to export symbol and component properties.



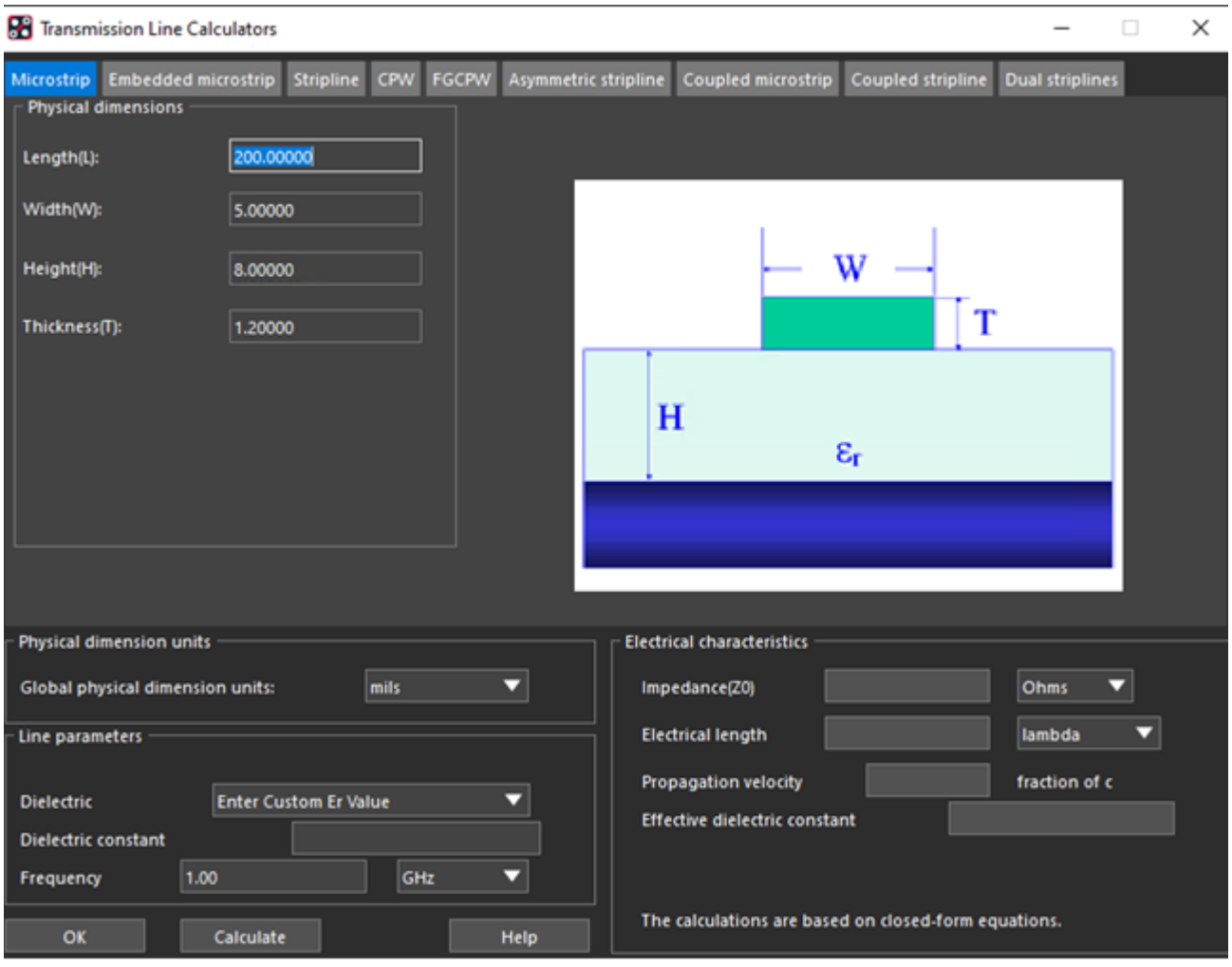
On import, the properties are applied to the listed object types. You can apply the properties to one or all instances of a component in a design.

- Configure the default state of derive assignment option

  To set the default state of derive assignment related options in wizards, configure the *icp_derive_assign_default_value* under *Ic_packaging* in User Preferences Editor.

Transmission Line Calculators in Allegro X Advanced Package Designer

Now, you can access Transmission Line Calculators (*Analyze – Transmission Line Calculator*) from Allegro X Advanced Package Designer.



You can use Transmission Line Calculators to calculate the correct stackup material and width or spacing to meet any requirements that may be later entered in a constraint.

Use the calculators if you need to test a quick spacing or width as per the impedance value. Use simulators for more precise results.

Quick Access to Snap Window

You can now access all *Snap pick to* commands immediately by pressing `Shift` with right-click.

SKILL Support for Expanded Hole Checks

In this release `axlCNSSetSpacing` and `axlCNSSetSameNet` are updated to include constraint symbols to support expanded hole checks: Thru Via, BB Via, Microvia, and Pin Hole.

Creating Mechanical Devices using axlCreateDeviceFileTemplate

You can now create mechanical devices using `axlCreateDeviceFileTemplate`.

Allegro X Pulse and Allegro X EDM

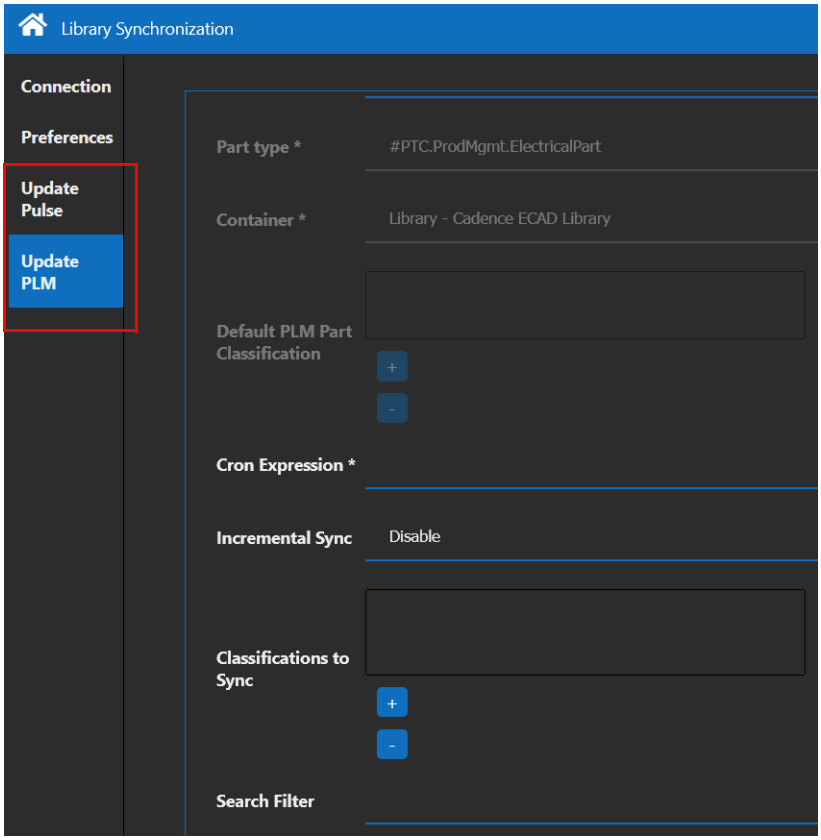
This section describes the following new features and enhancements in Allegro® X Pulse and Allegro® X Engineering Data Management (EDM) in release 23.1.

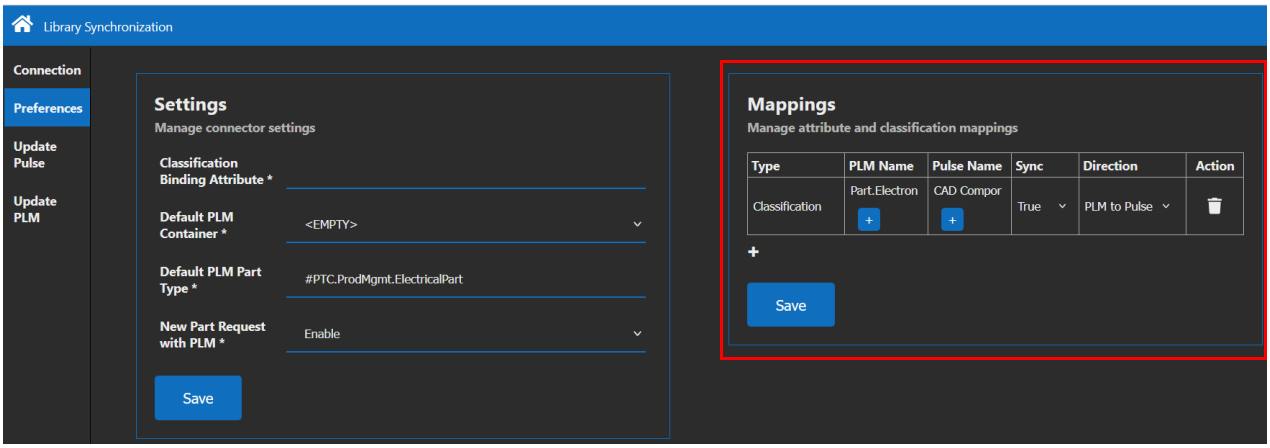
Two-way Synchronization between Allegro X EDM and PTC Windchill Data

Allegro X EDM library parts can be updated with changes in the Windchill part data. Conversely, Windchill parts can also be updated with the changes in the EDM library data starting with this release. To enable this two-way synchronization, the *Preferences* page of the Library Synchronization window provides:

- A mapping table to map the PTC Windchill attribute names to the Allegro EDM classification property names.

- A set of parameters to manage Windchill part metadata.





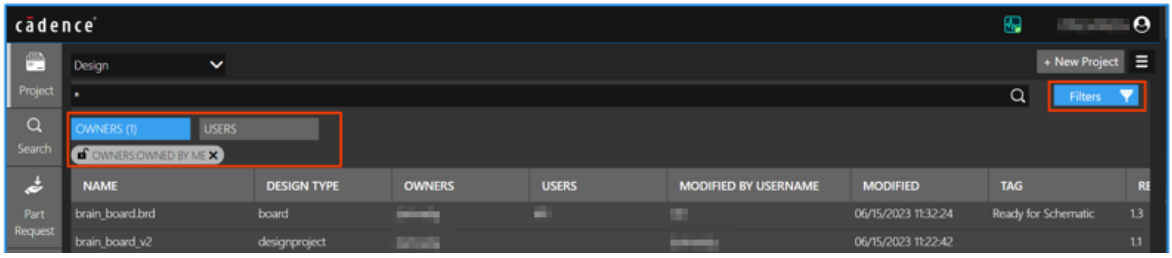
Related Documentation

- *Library Synchronization Between PLM Systems and Allegro X Pulse*

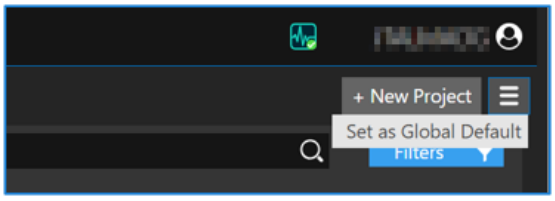
Enhancements in Pulse Web Dashboard

Enhancements in the web dashboard are available for users in the single-user and multi-user environments of System Capture. The changes are as follows:

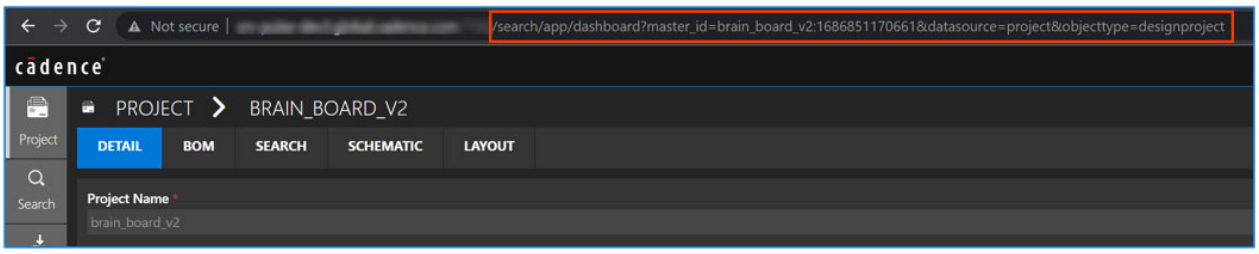
- Additional filters, *Owned by me* and *shared with me,* enable easier viewing of projects and designs.



- Save column visibility, the column order, and a filter for a project list as the global default for administrators.

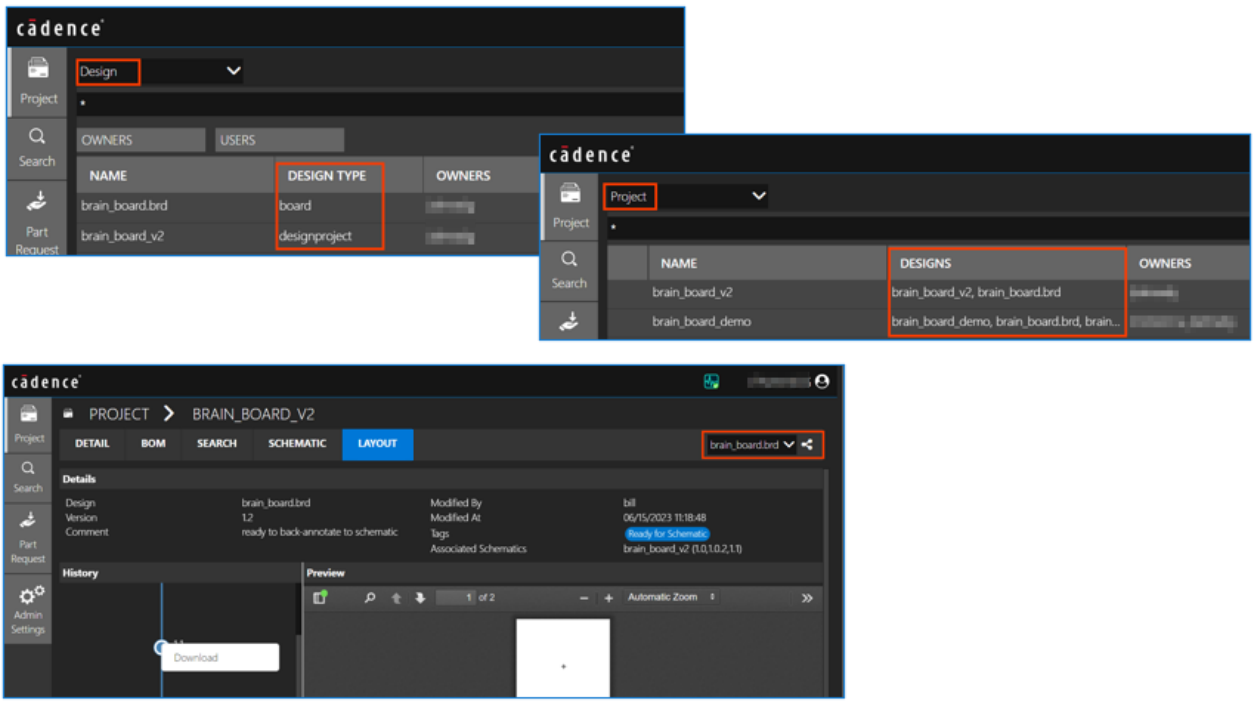


- A project-specific URL is now available for easy bookmarking. This makes it easy to quickly open a design or layout in a web browser and view its details or share it.



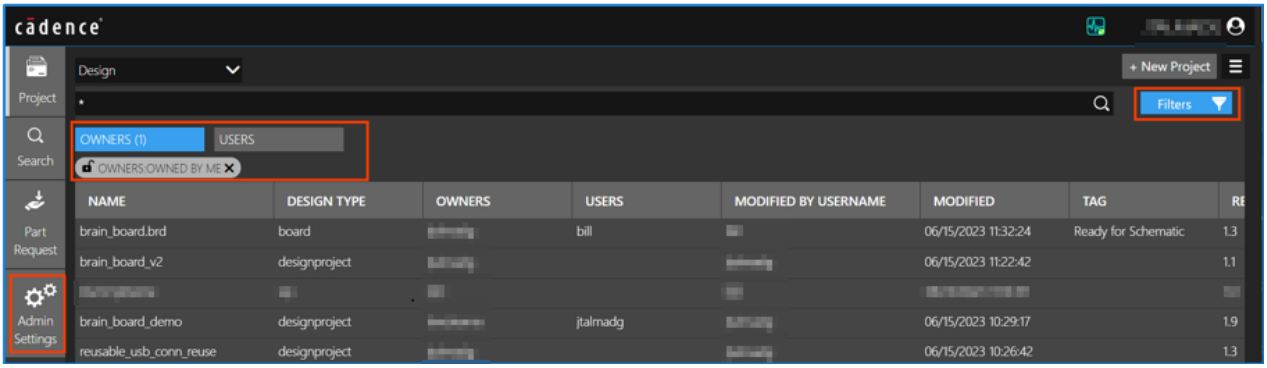
- The *Part Search* tab on the left of the web page has been renamed as *Search*.
- There is a *Project* and *Design* view. The *Project* view displays project containers and the designs contained within. The *Design* view shows all Pulse-managed designs, which

includes schematics and layouts. This enables layout visibility in the *Layout* tab on double-clicking a project in the *Design* or *Project* list.



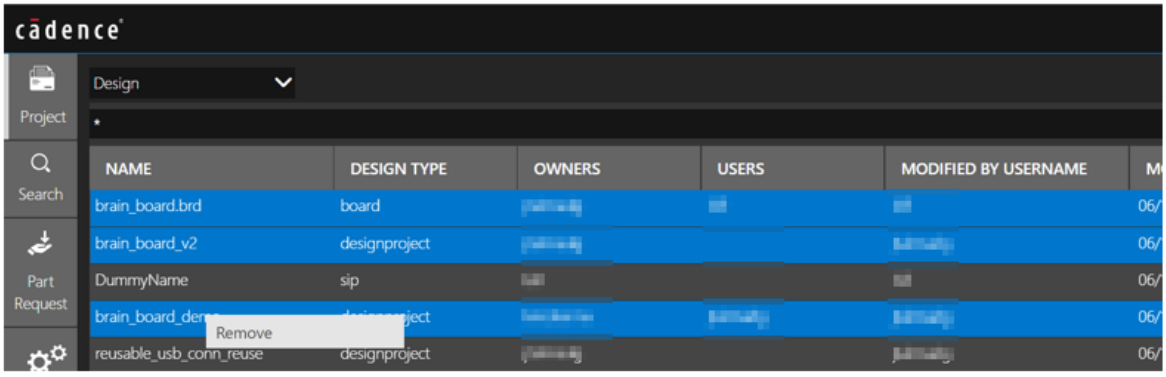
You can share a layout, view the layout versions, and download layout versions from *Version Control*.

- The administrator tasks have moved to the left side of the web page and are no longer available under the user profile icon.



- Instead of clicking, you must now double-click to open a project or design from the list. Click now selects a project or design instead of opening it.

- You can multiselect designs and remove them in one go from the *Design* list.

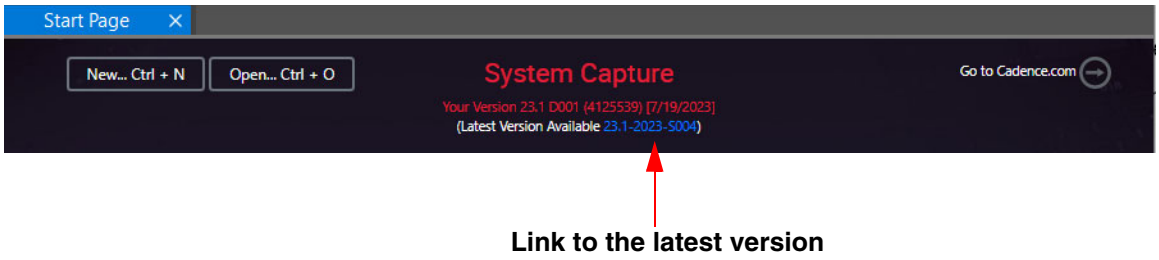


Allegro X System Capture

This section describes the following enhancements and new features in Allegro® X System Capture in release 23.1.

Update Available Notification

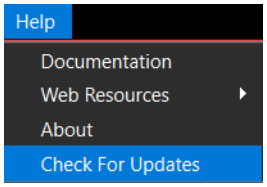
The *Start Page* shows the latest version available for System Capture. Click this link to download the newer version. In case you are in an enterprise setup, or you do not have the required permissions, downloading and updating the installed version might require administrator support.



Link to the latest version

The version numbers in your installation might be different from the ones in the image.

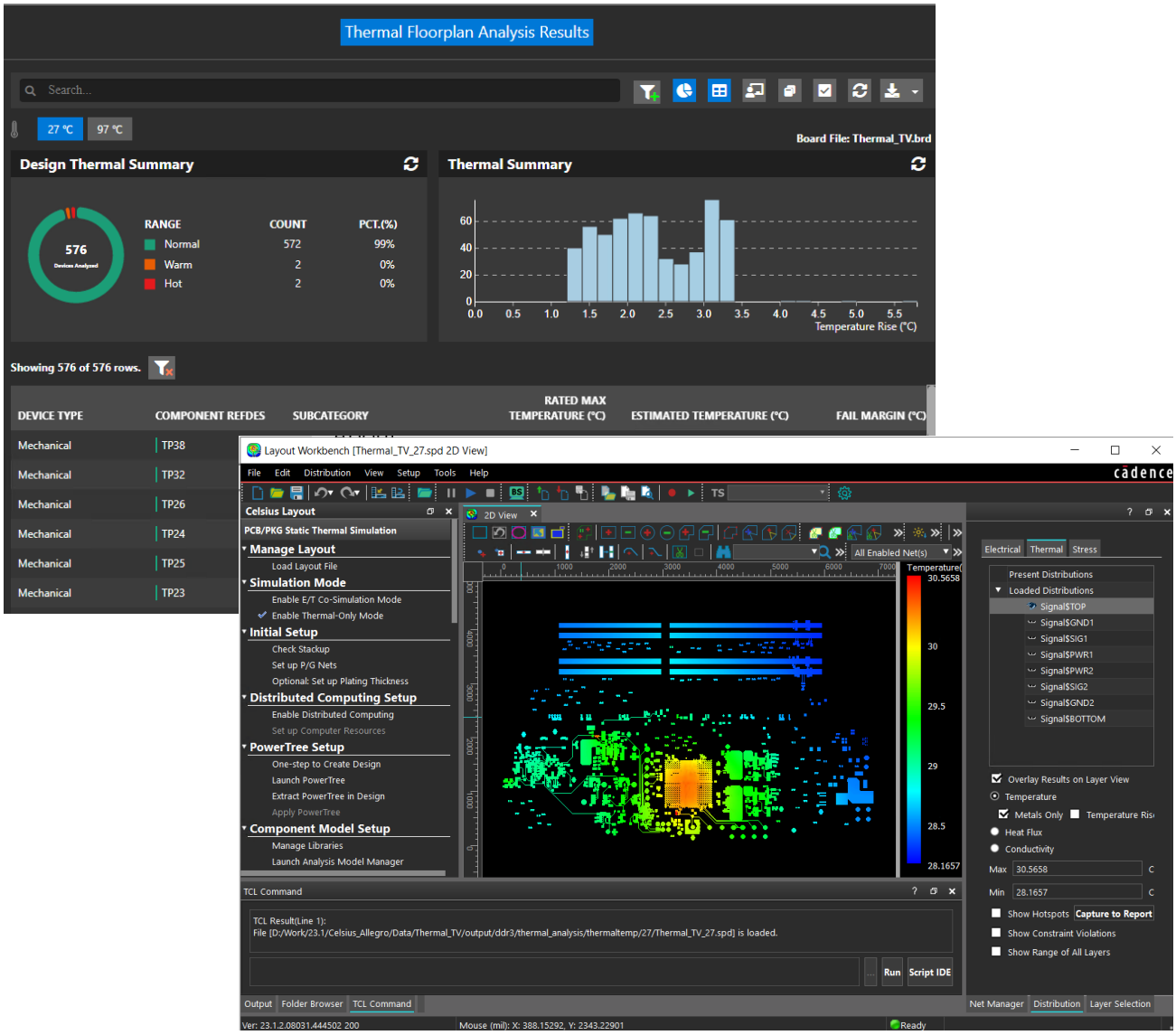
A new *Help – Check for Updates* option is also added to check if newer updates are available.



Thermal Analysis and Celsius Integration

Generating a thermal floorplan for a board file is now possible in System Capture. The thermal analysis results help in estimating the life of a PCB design and improved placement of components early in the design cycle.

Access to Celsius Thermal Solver has also been provided from the Electrical Analysis dashboard.

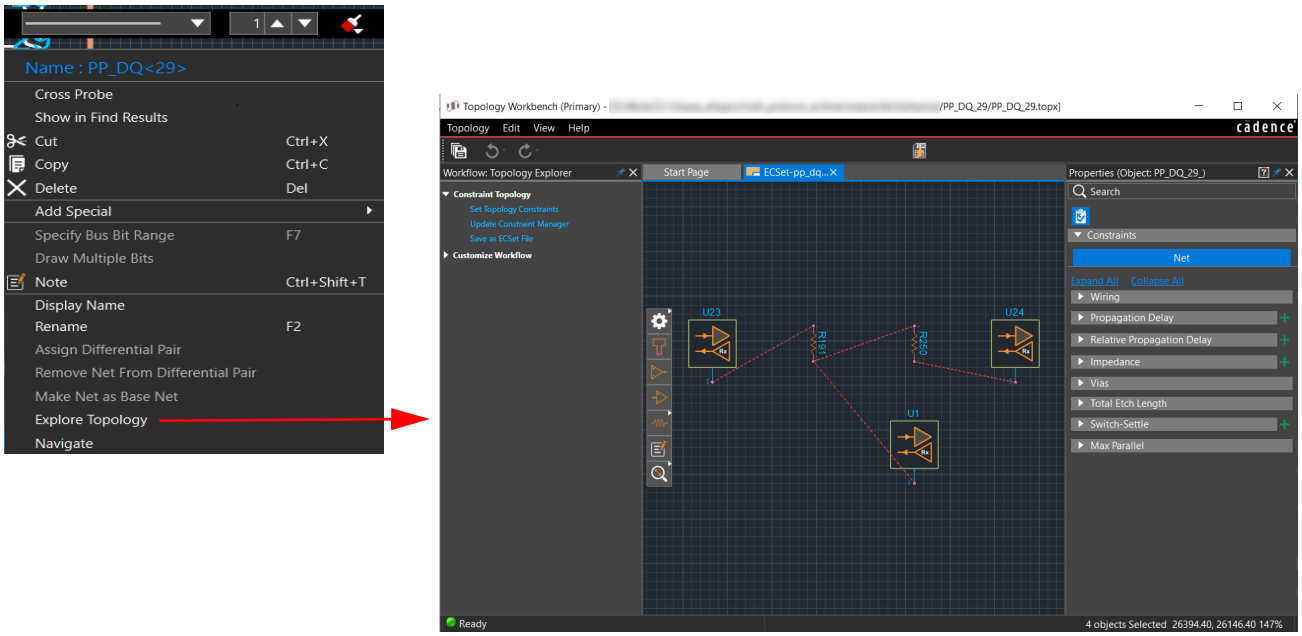


Related Documentation

- Thermal Analysis with Celsius Thermal Solver

Topology Workbench Integration

Topology Workbench has replaced Signal Explorer for analyzing the signal integrity of hi-speed nets at the schematic, floorplan, and layout stages. All the Constraint Manager-based ECSet creation and modification flows as well as simulation flows continue to be supported. You can launch Topology Workbench directly from System Capture Canvas for a single net or XNet or from Constraint Manager.



Related Documentation

- Extracting Topology in Topology Workbench

New Analysis Modes Available in Design Integrity

Design Integrity has been extended to include two new analyses:

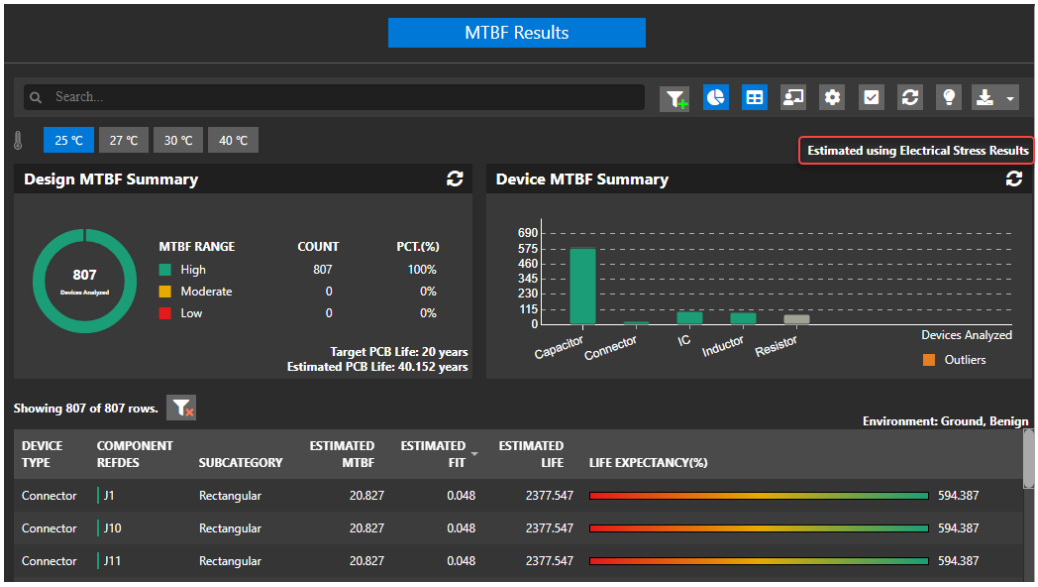
- MTBF (Mean Time Between Failure) Analysis
- Power Topology Analysis

MTBF (Mean Time Between Failure) Analysis

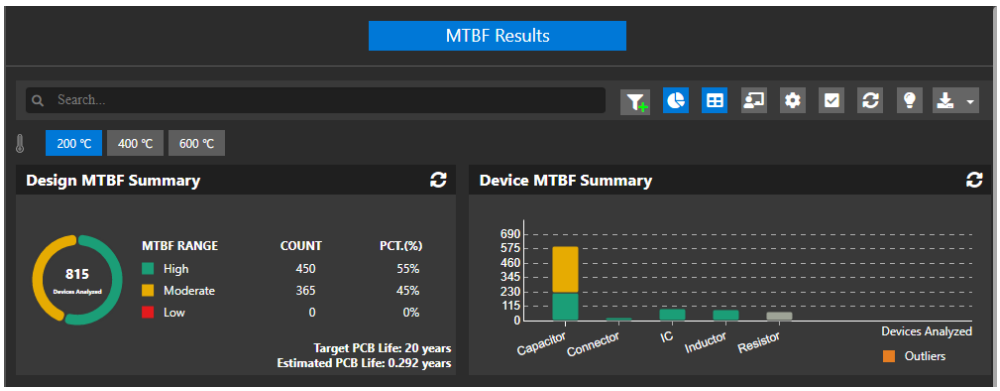
System Capture is enhanced to support MTBF analysis on a design to estimate the performance and safety of electrical, mechanical, and electro-mechanical parts. MTBF analysis is available with the following licenses:

- `Allegro X Designer`
- `Allegro X Designer Plus`
- `Allegro X Venture`

MTBF results can be calculated with or without using the electrical stress data generated in the last run.



You can also configure the ambient temperatures used for MTBF analysis.



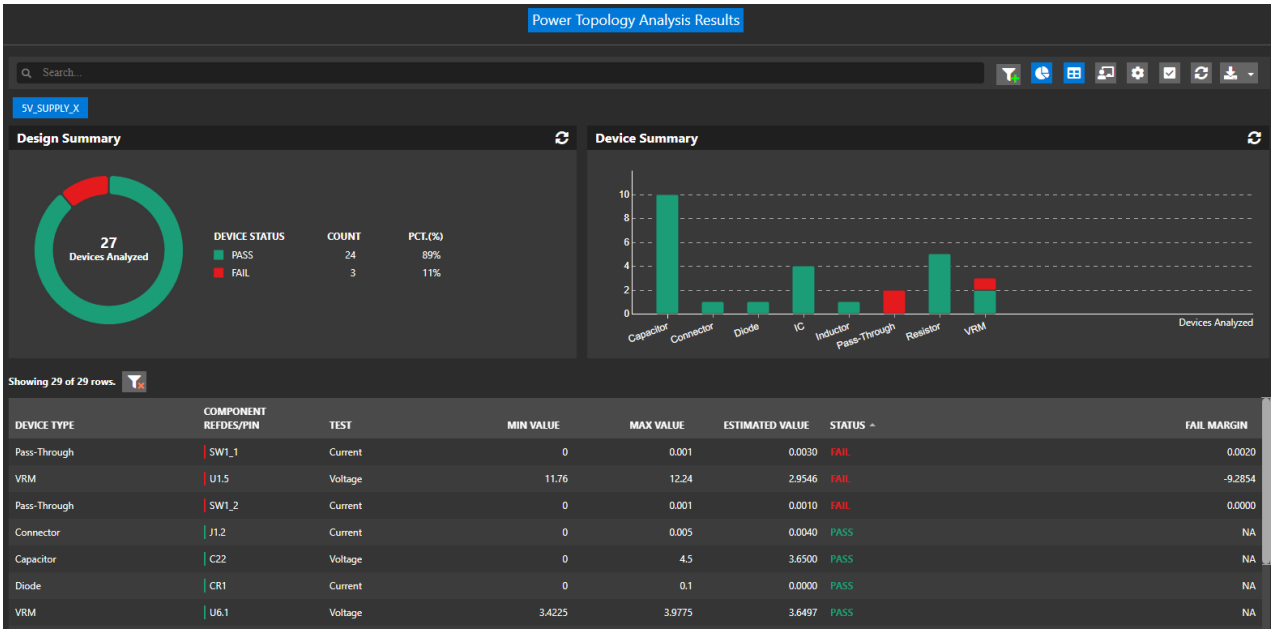
Related Documentation

- MTBF Analysis

Power Topology Analysis

Power Topology analysis sets up a power distribution network on the schematic and estimates the DC power consumption by the PCB design components. This enables the verification of all the components in a design in the early stages of design development. Power Topology analysis is available with the following licenses:

- `Allegro X Designer`
- `Allegro X Designer Plus`
- `Allegro X Venture`

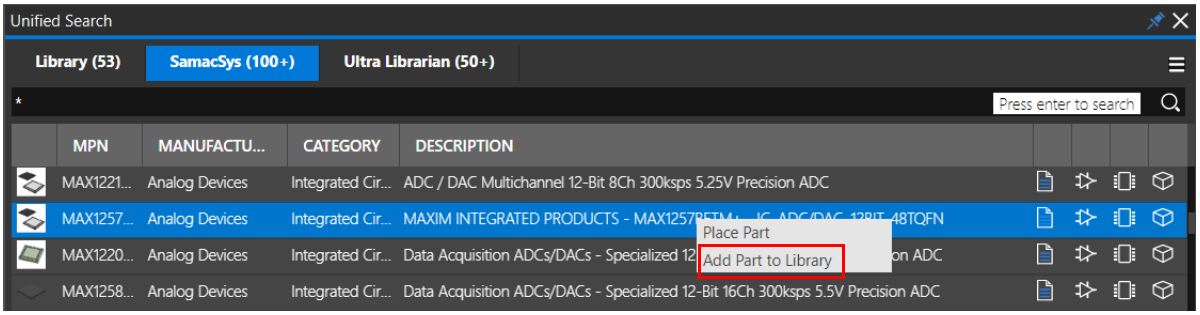


Related Documentation

- Power Topology Analysis

Adding Parts from External Content Providers to Libraries

In addition to adding parts from external content providers, such as *SamacSys* or *Ultra Librarian,* directly into a design, *Unified Search* now supports adding parts to libraries and then using them in your designs.



Related Documentation

- Adding Parts from External Content Providers

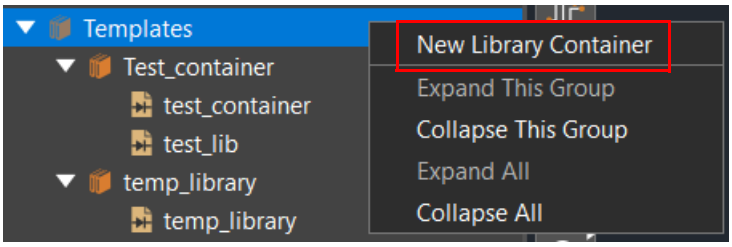
Library Authoring Enhancements

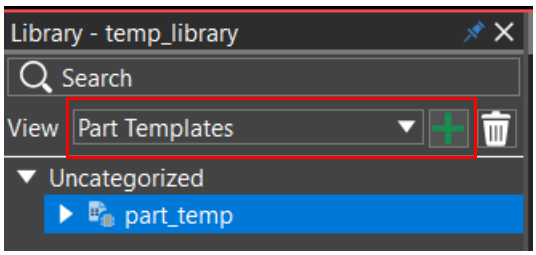
The following new features are introduced in this release for Allegro Unified library authoring:

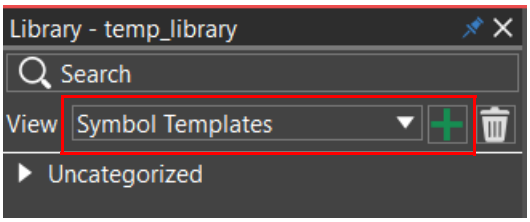
- Templates Introduced for Libraries
- Creating Categories in a Library
- Edit Multiple Parts in a Spreadsheet
- Support for Custom Shapes and Pin Shapes
- Enhanced Validation Checks Added

Templates Introduced for Libraries

You can create a new template library container under the *Templates* node, and create a new part or symbol template in this container. In addition to the default templates available for creating a part or a symbol, custom part and symbol templates are also available.



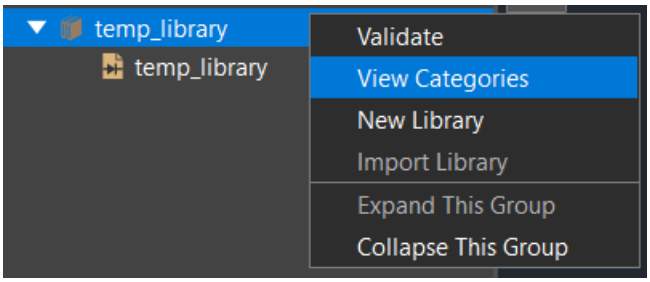


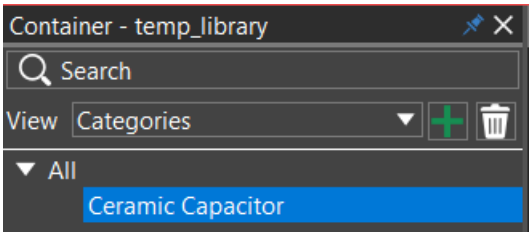


Creating Categories in a Library

New categories and subcategories are available in the template library that improve component searching. For example, you can categorize a schematic model, resistor, as

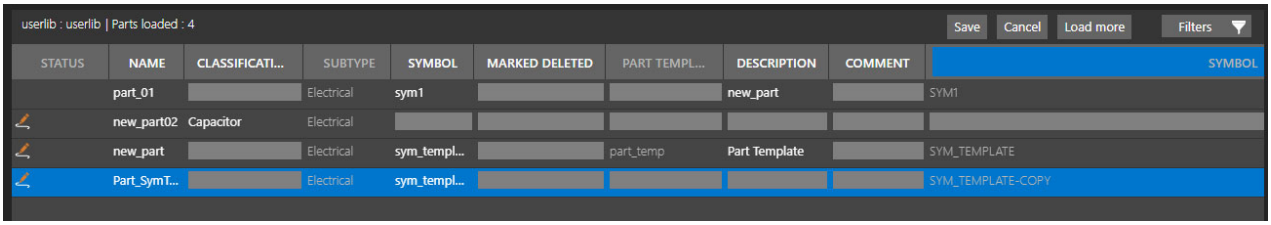
Discrete, which can be sub-classified as *Resistor*. You can search for a keyword, *Discrete* or *Resistor*, and assign it to a part or a symbol.





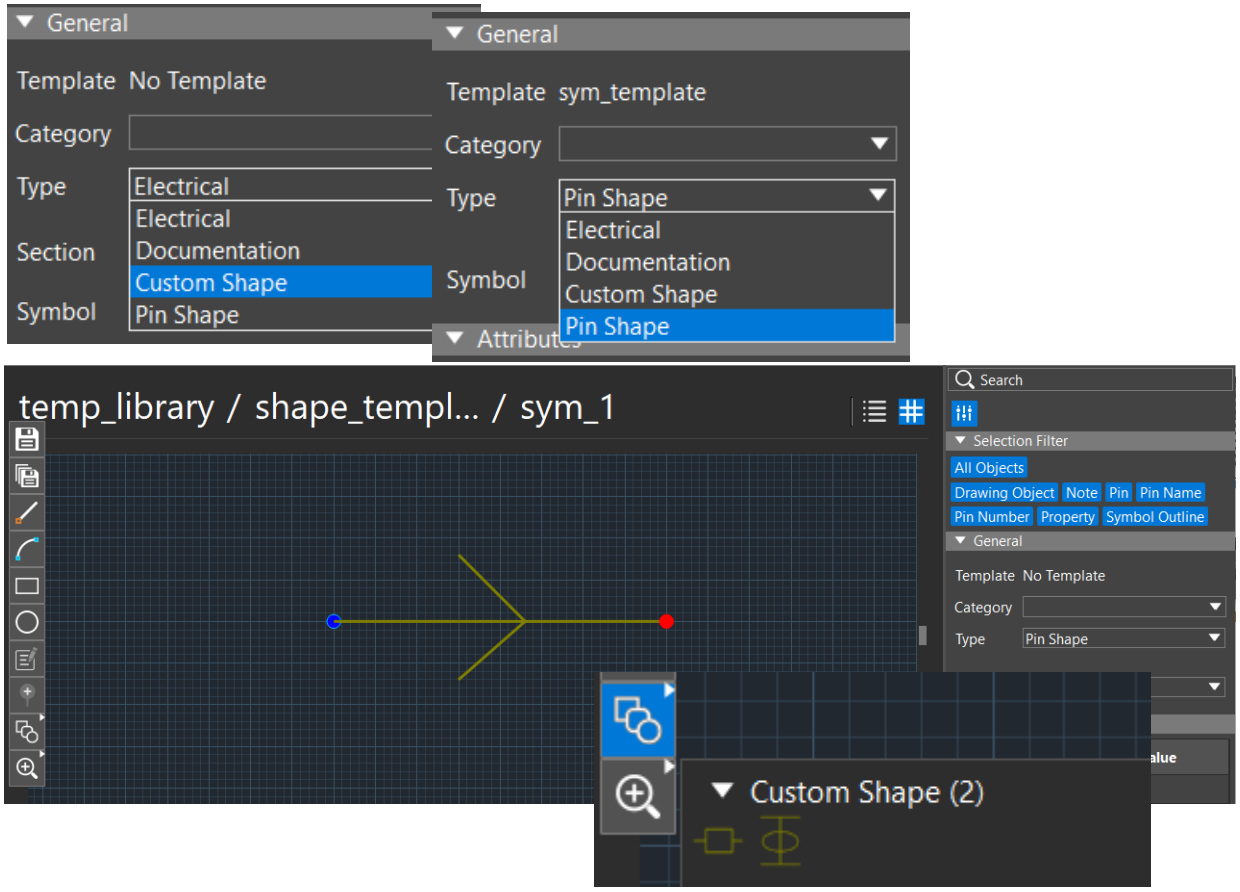
Edit Multiple Parts in a Spreadsheet

Modifying part names, descriptions, and properties is now simpler in the spreadsheet view for part editing. You can edit multiple part properties, schematic model, footprint, simulation model, datasheets, and other columns in this spreadsheet view.



Support for Custom Shapes and Pin Shapes

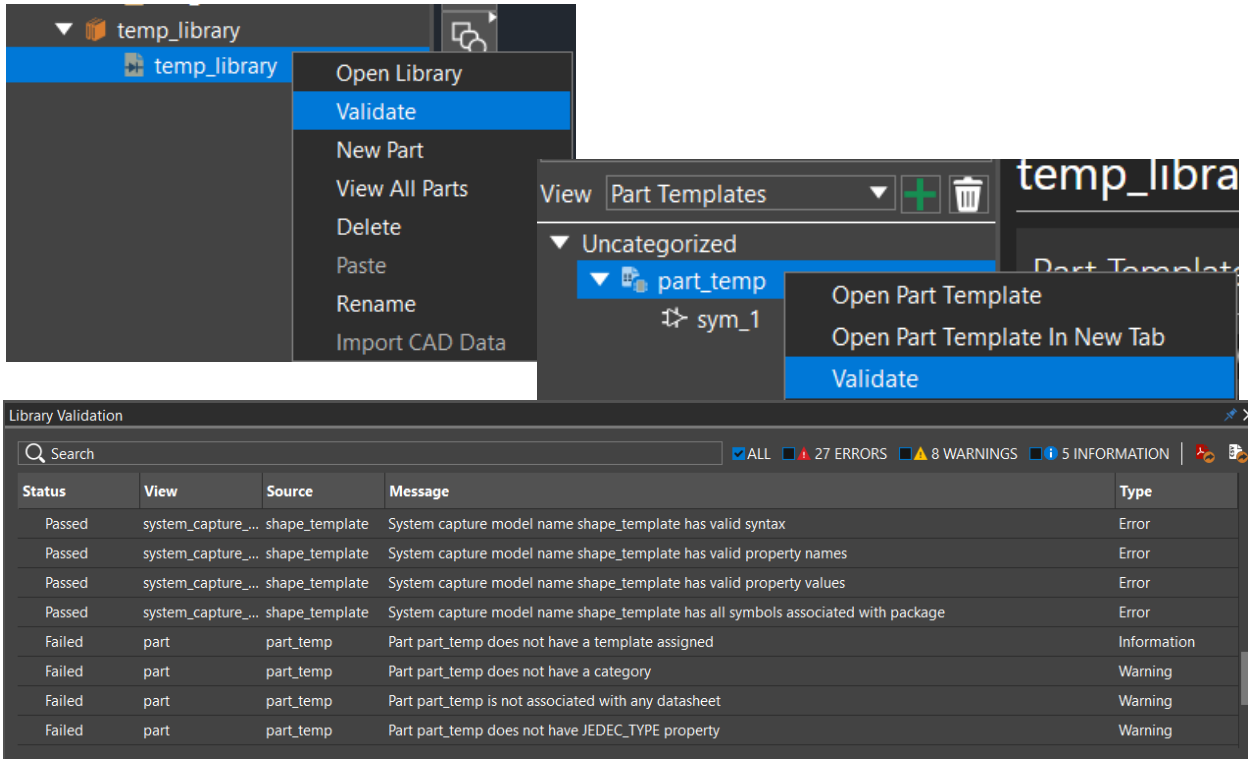
You can create a new custom shape or a pin shape under a template library and attach it to a pin or the complete symbol. This feature is available for projects based on Allegro Unified or DE-HDL libraries.



Enhanced Validation Checks Added

Validate libraries and data models including parts, schematic models, footprints, and data sheets to avoid common errors in a design with the *Library Validation* window. Libraries,

parts, and schematic models are validated based on the rules defined in *Library Audit Settings*.



Related Documentation

- Library Authoring and Editing in Allegro X System Capture

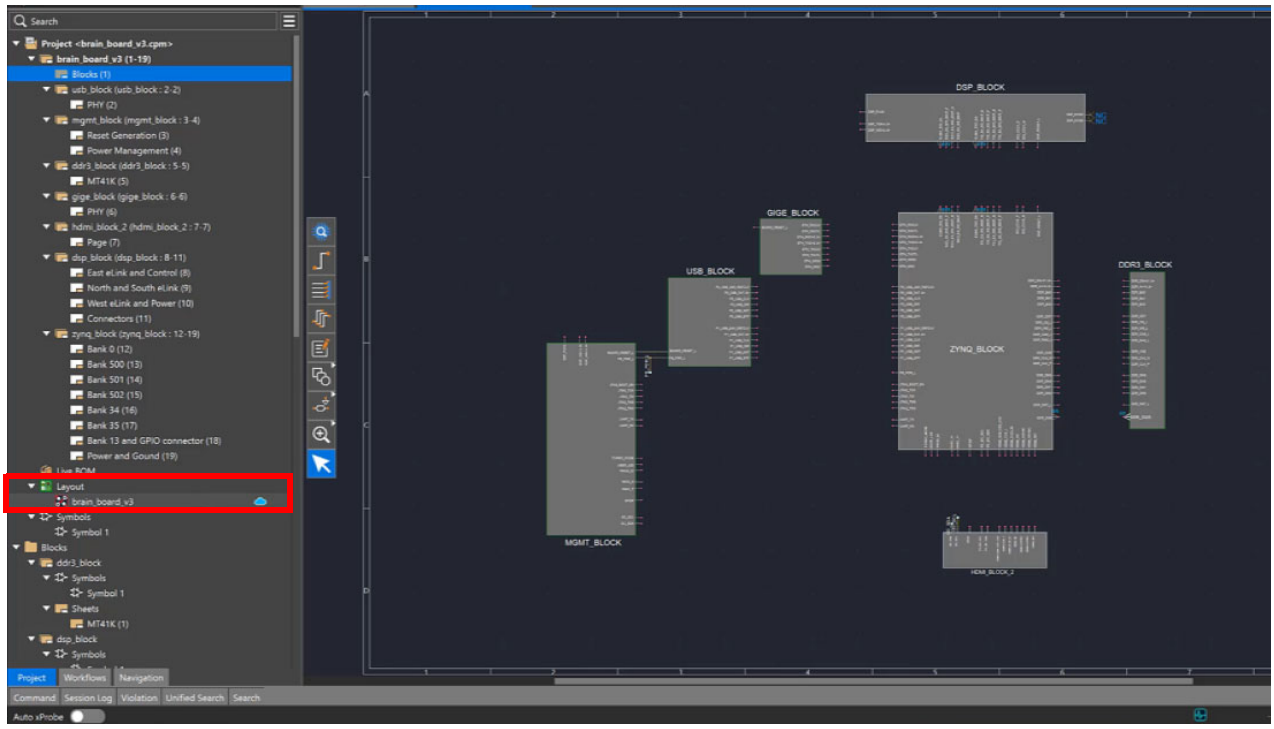
New Features in the Multi-User Environment

When connected to a remote Pulse server, the following additional features are available:

- Managed Layouts in Project Explorer
- Pulse Web Dashboard Updates
- Pulse Status Icons
- Comparing Versions
- Working in the Offline Mode
- Design Search and Reuse

Managed Layouts in Project Explorer

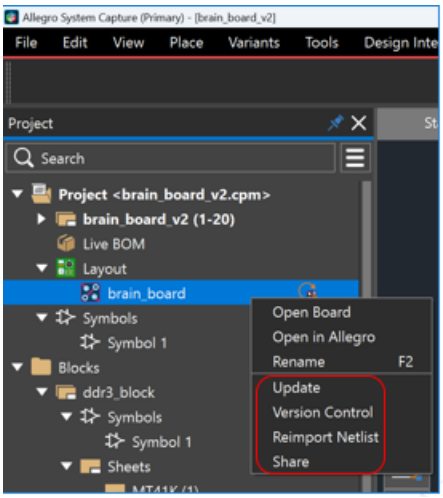
System Capture users in a multi-user environment can stay updated with the latest changes in layouts associated with schematics. Pulse-managed layouts include boards, packages, and modules, and are displayed in Project Explorer, if you have read or edit permissions for the layout files.



Tooltips displayed on hovering the mouse over layouts display the layout status, such as:

- Sync status with the associated schematic
- If a new revision is available
- Downloaded layouts that have been removed from the design in the Pulse web dashboard

Additional tasks are available from the context menu for Pulse-managed layouts, as shown in the following image.



Related Documentation

- Design Data Management in Allegro X System Capture

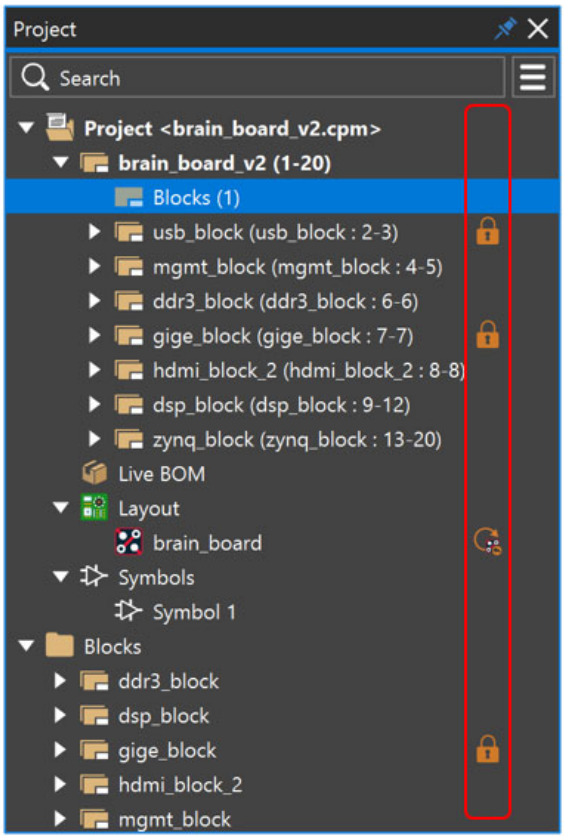
Pulse Web Dashboard Updates

Enhancements in the web dashboard are available in the single-user and multi-user environments of System Capture.

For a detailed list of the enhancements, see Enhancements in Pulse Web Dashboard on page 68.

Pulse Status Icons

The Pulse status icons, which provide notifications for team design, layout, and design reuse are now on the right side of the Project explorer pane. This enables easy viewing of the object type in the project.

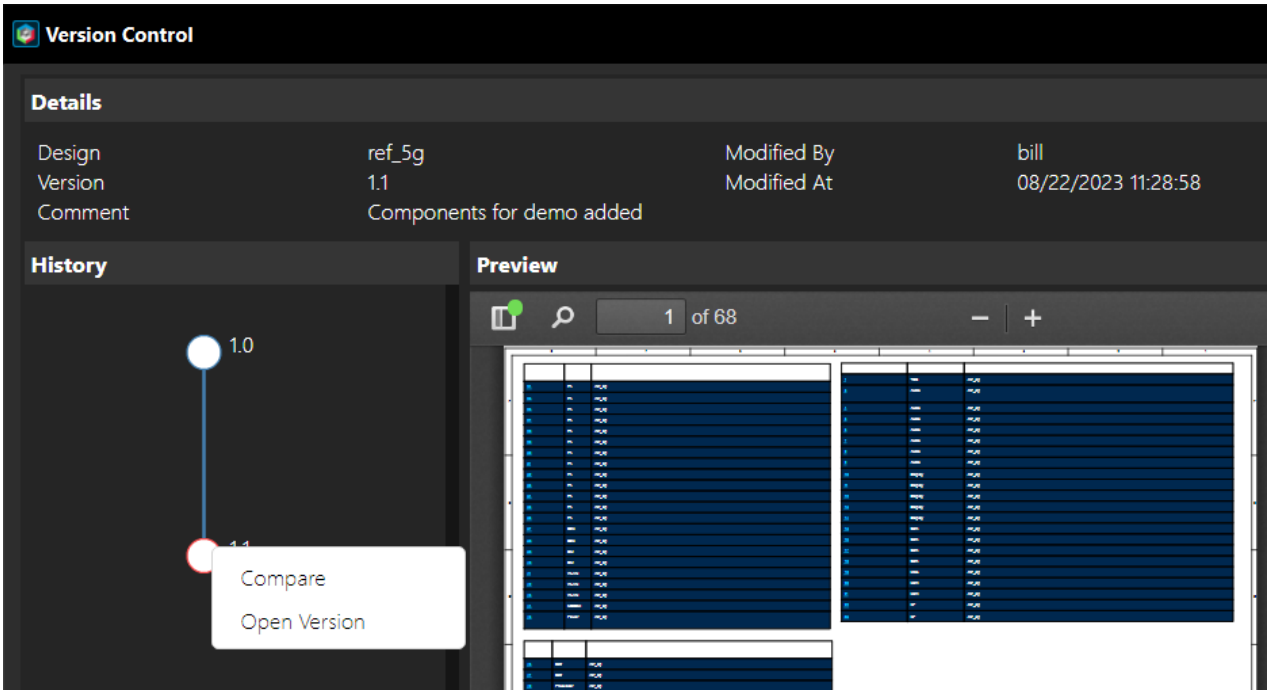


Comparing Versions

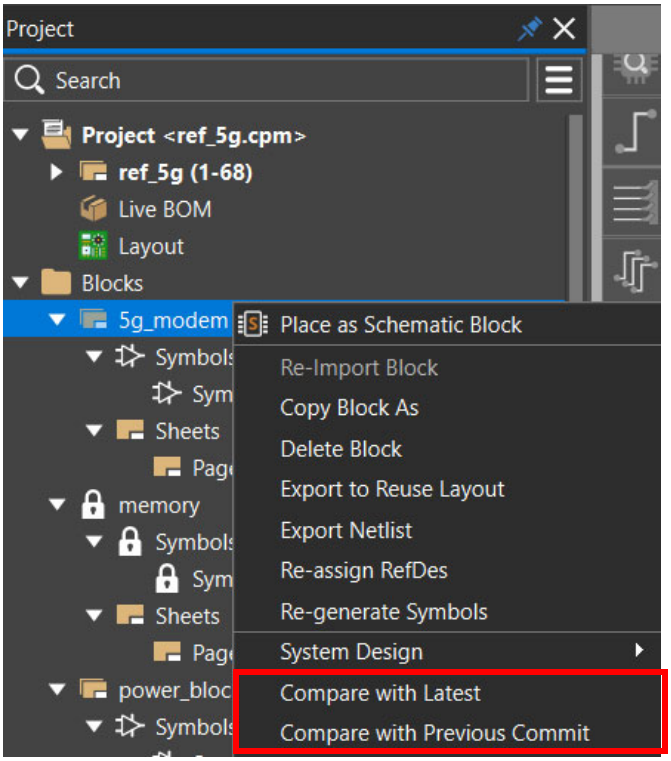
To enable easier decision-making on whether to accept a team design update, you can now compare:

- Two design versions in *Version Control*.

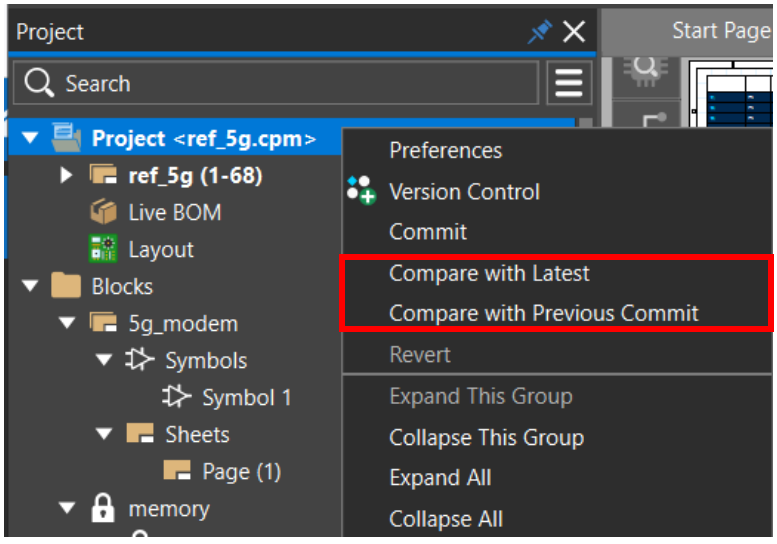
Right-click the first version and select *Compare* then click the second version.



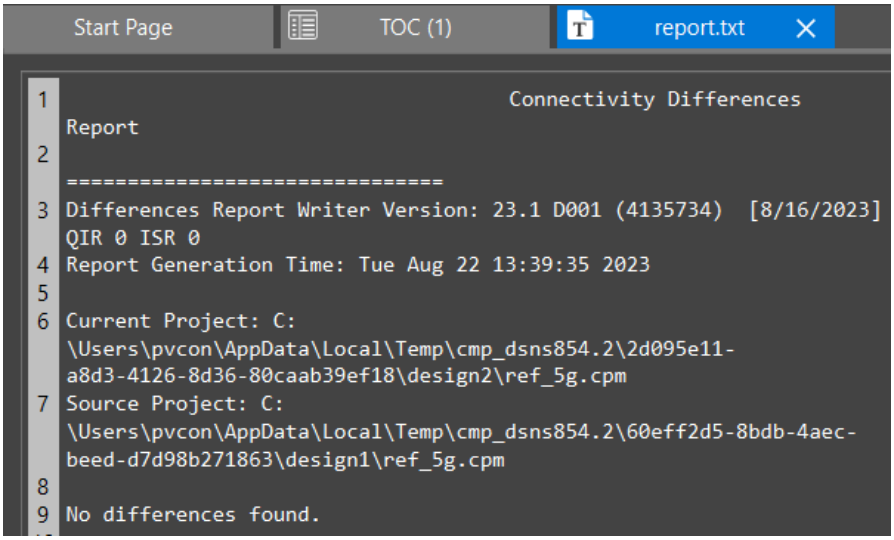
- Individual blocks with the previous or latest commit versions.



- The design with the latest version or any earlier version.



The differences are displayed in a new tab.



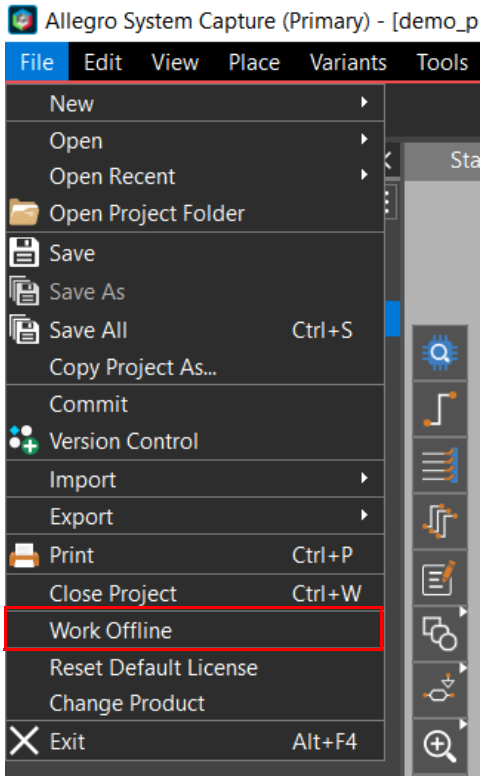
Related Documentation

- Comparing Designs

Working in the Offline Mode

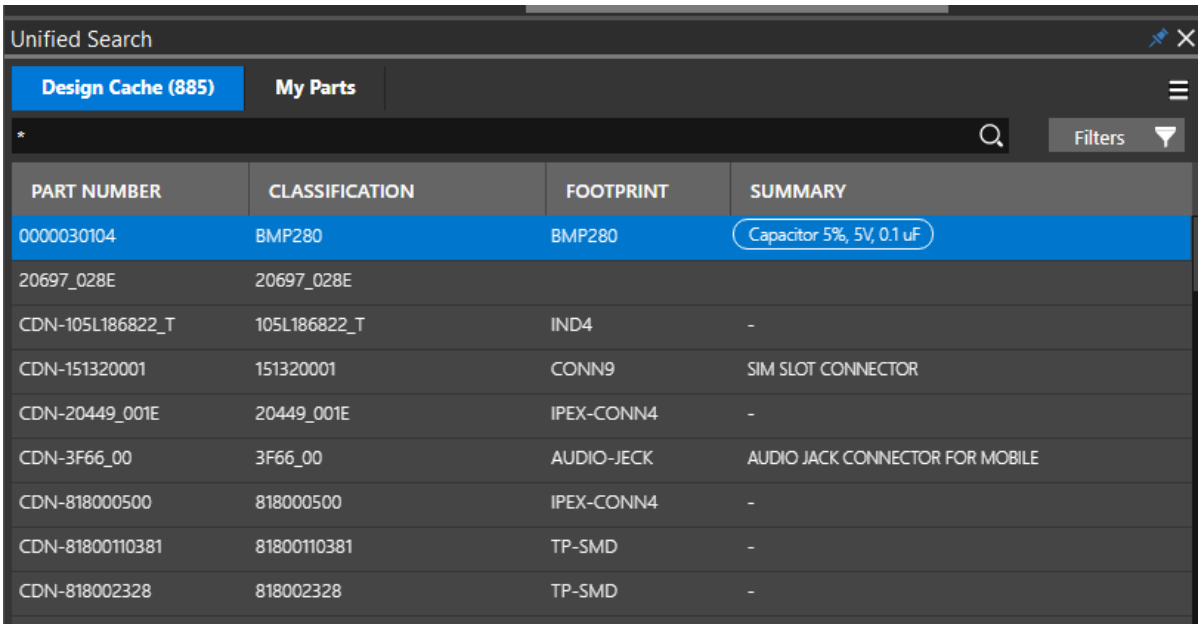
If network connectivity is slow or the Pulse server is temporarily unavailable, users in a multi-user environment can disconnect from the Allegro Pulse server services and work in the

offline mode. This ensures uninterrupted work using parts in the design cache. You can connect to the server again, when available.



The offline mode is only supported for Allegro System Capture projects with Design Entry HDL or OrCAD Capture libraries.

In the offline mode, you can only work on pages and blocks that you have explicitly locked before disconnecting from the Pulse server. Only parts cached in your local libraries are available in the offline mode in a *Design Cache* tab in Unified Search.



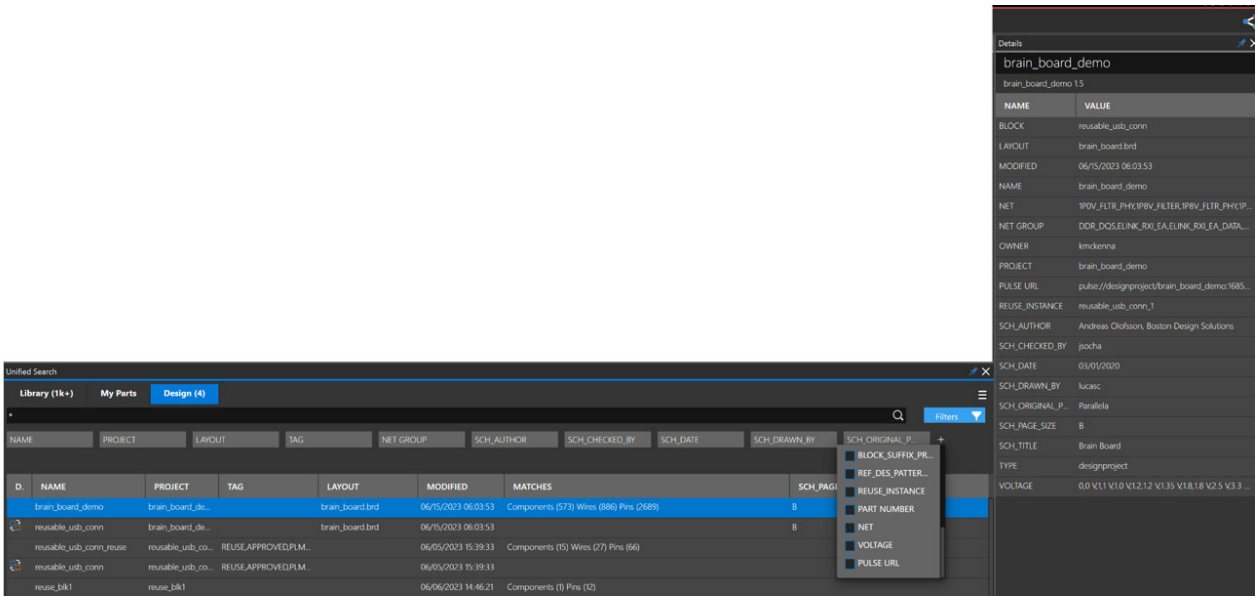
Related Documentation

- Disconnecting from Pulse Server

Design Search and Reuse

Unified Search supports searching data across designs, and within design metadata. A new tab, *Design* has been introduced in the multi-user environment. Search results display data

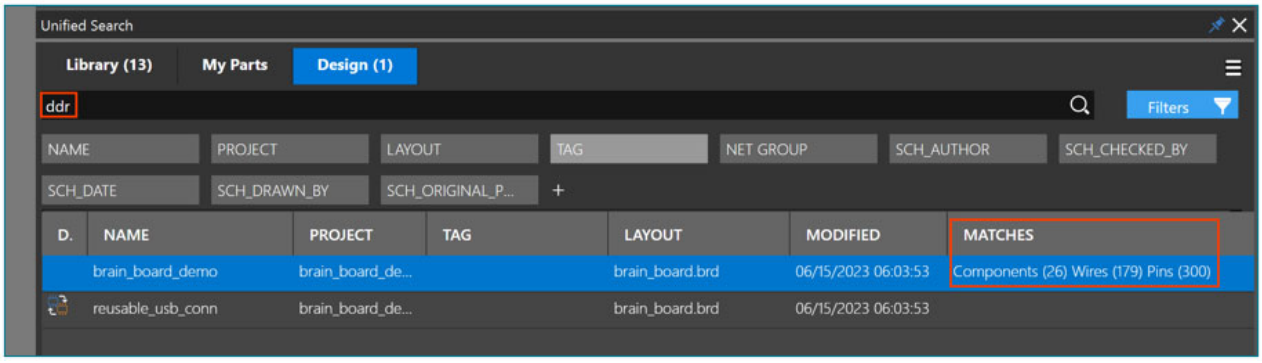
from the latest committed versions of the designs available on the common server. You can also perform a parametric search of a design row in the *Details* pane.



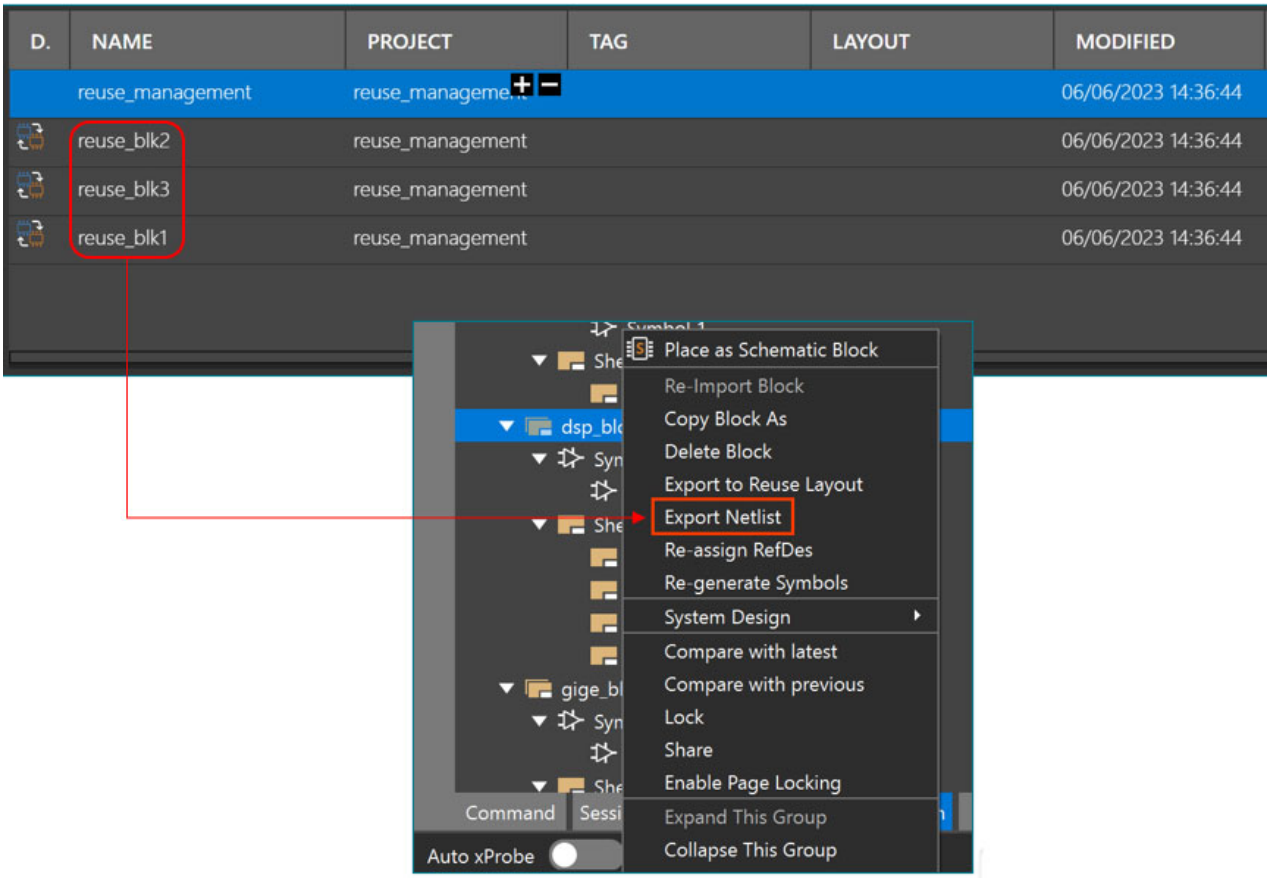
Searchable data includes:

- Pulse metadata: Content in the project details form, version, the last modified date, design owner names, users with read-only access to a design, commit tags, comments, the Pulse URL
- Design information: Nets, NetGroups, buses, components, pins, voltages, CUSTOMVARs, variant names, block attributes, and layouts associated with schematics

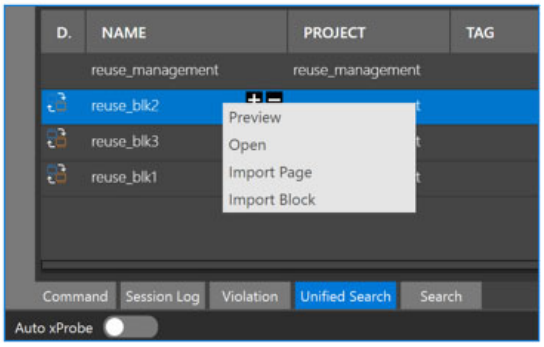
  Search results are aggregated into matches.



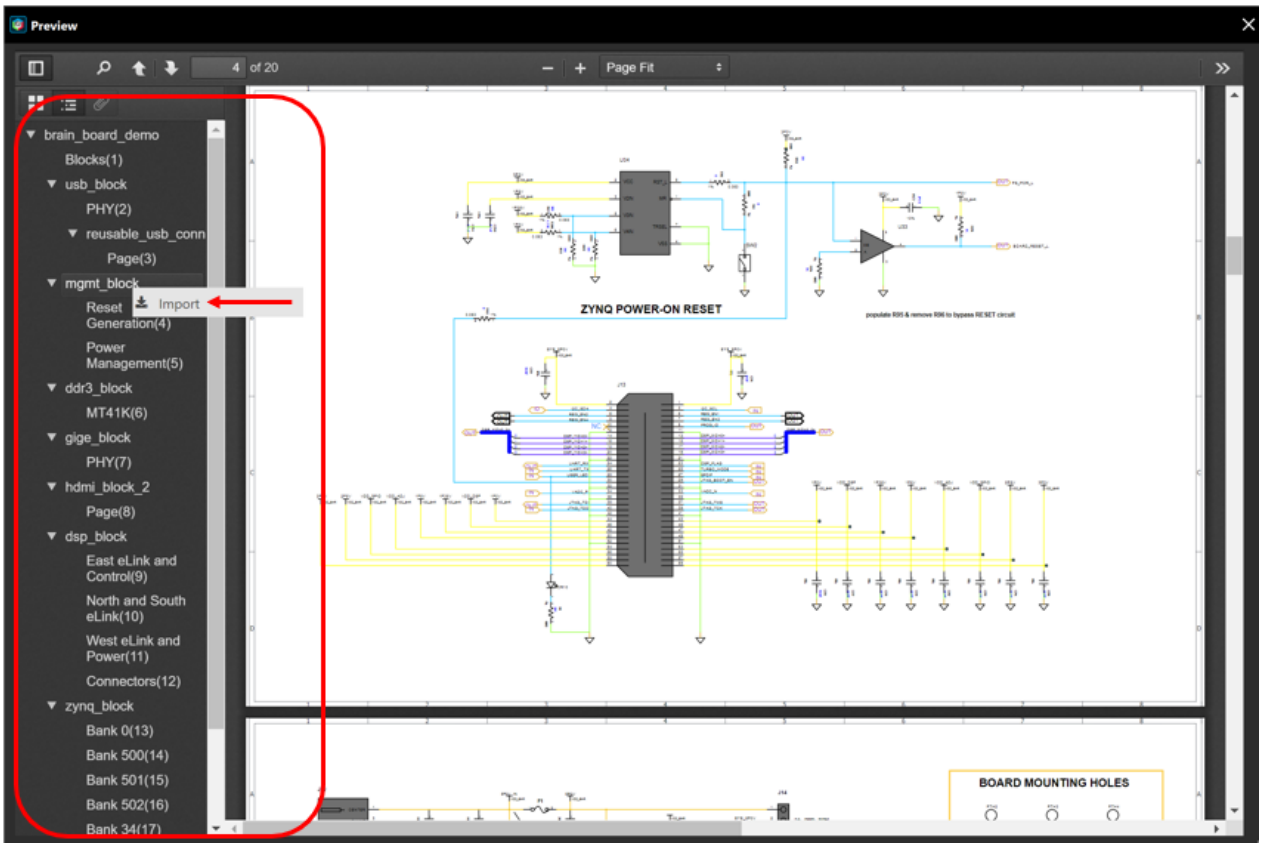
To enable easy reuse of a design, blocks where netlists are exported for reuse are identified with an icon in the first column.



With read-only access to a design, you can preview it, import blocks or pages, and open a design in a new System Capture instance. You can also copy elements of one design to another across two System Capture instances.

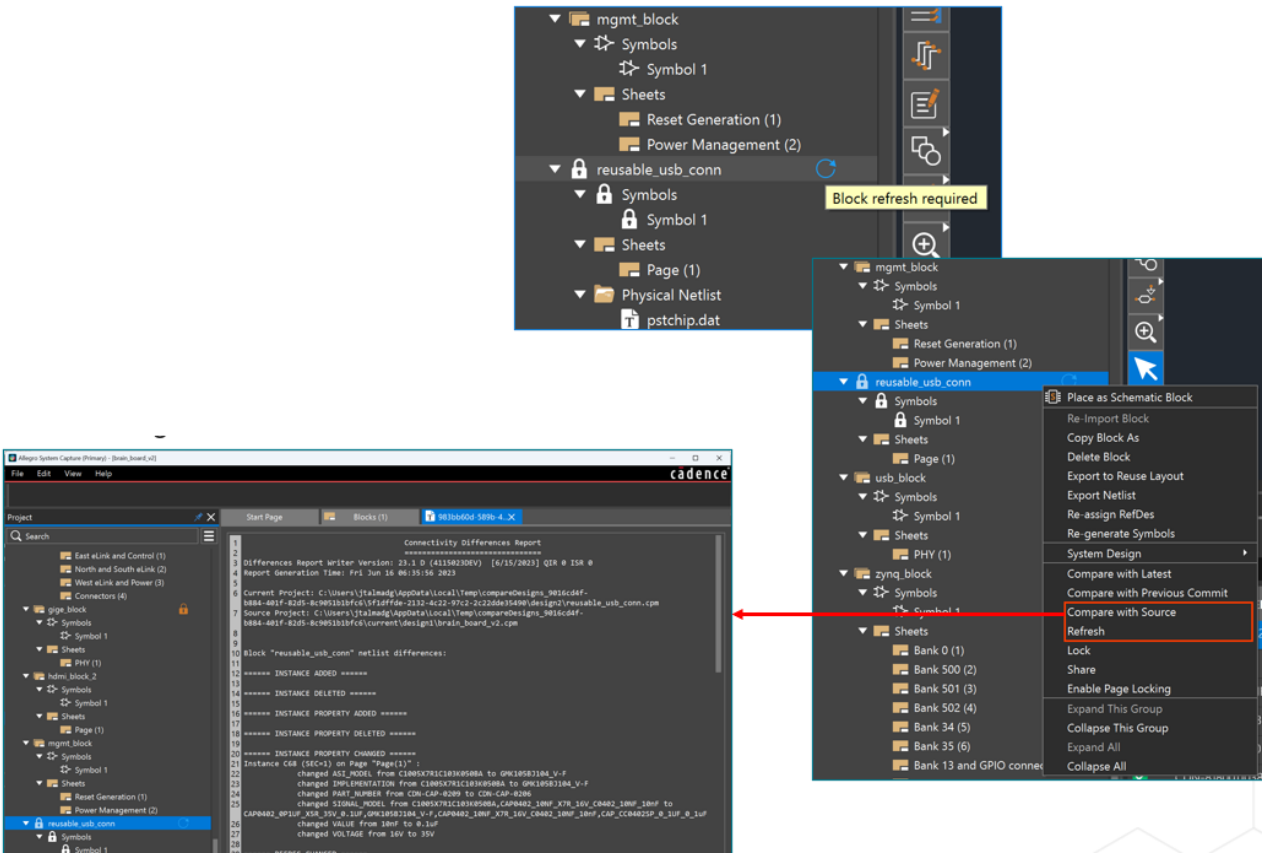


The *Preview* search result includes a PDF with hierarchical navigation. You can right-click an item in the hierarchy navigation, and import a block or page.



When a source design is committed and a change in it impacts a reused block, System Capture displays reuse update notifications for the blocks. You can view the differences to

assess the impact and click *Refresh* to update your design with the latest version of the reused block.



Related Documentation

- Searching for Designs for Reuse

AWR MWO-Allegro RF Design Flow

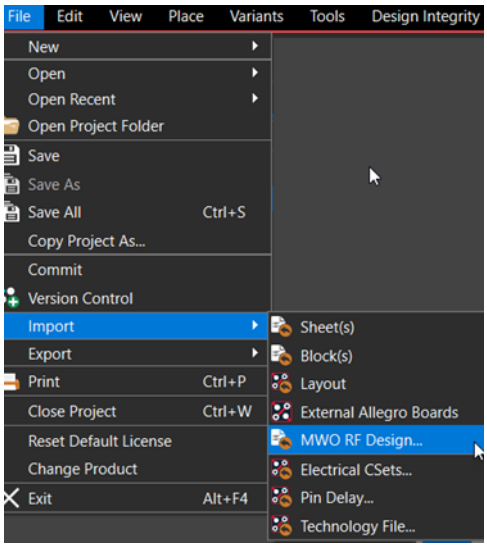
Important

This is currently a limited-release feature that is available only Windows. To enable the flow, create an environment variable `MWO_ALLEGRO` and set it to `1`.

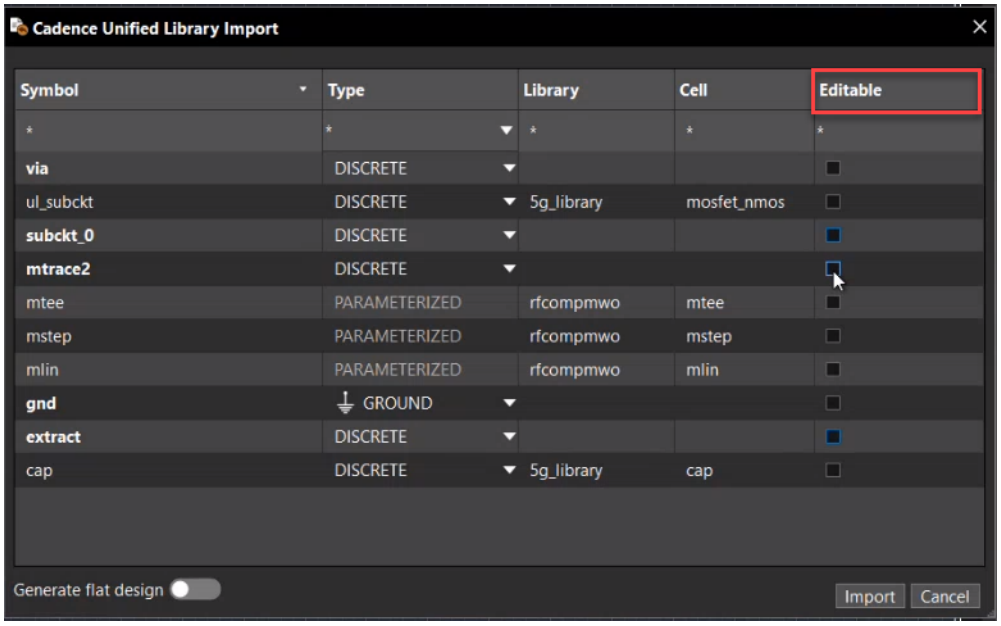
The integration of AWR® Microwave Office® (AWR MWO) and Allegro® PCB Design applications provides a way to create complex PCBs with RF design. Release 23.1 is compatible with MWO 17.03 version.

Enhancements in this release include the following:

- Single container import from AWR MWO into System Capture.



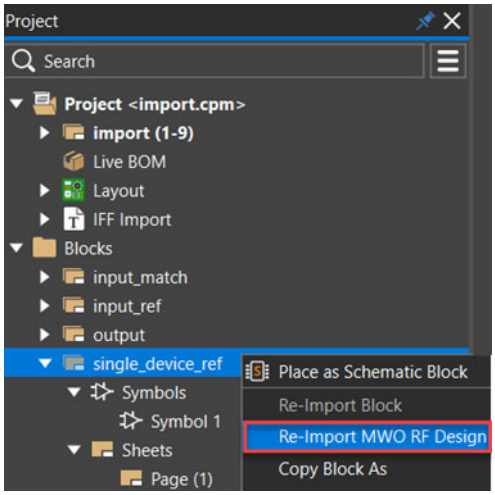
- Multi-primitives in the scope of components in the RFIP transfer flow.



- Unmapped components from a single container are no longer locked and can be replaced with components from an Allegro library. This enables the use of split, symmetric, and asymmetric parts.
- Import RFIP into existing non-RF schematic

A single container can be imported into an existing schematic. This allows an RF block to be reused both in the logical design as well as in the layout.

- Re-import support added for RF blocks.



Related Documentation

- Importing RF Design in Allegro System Capture

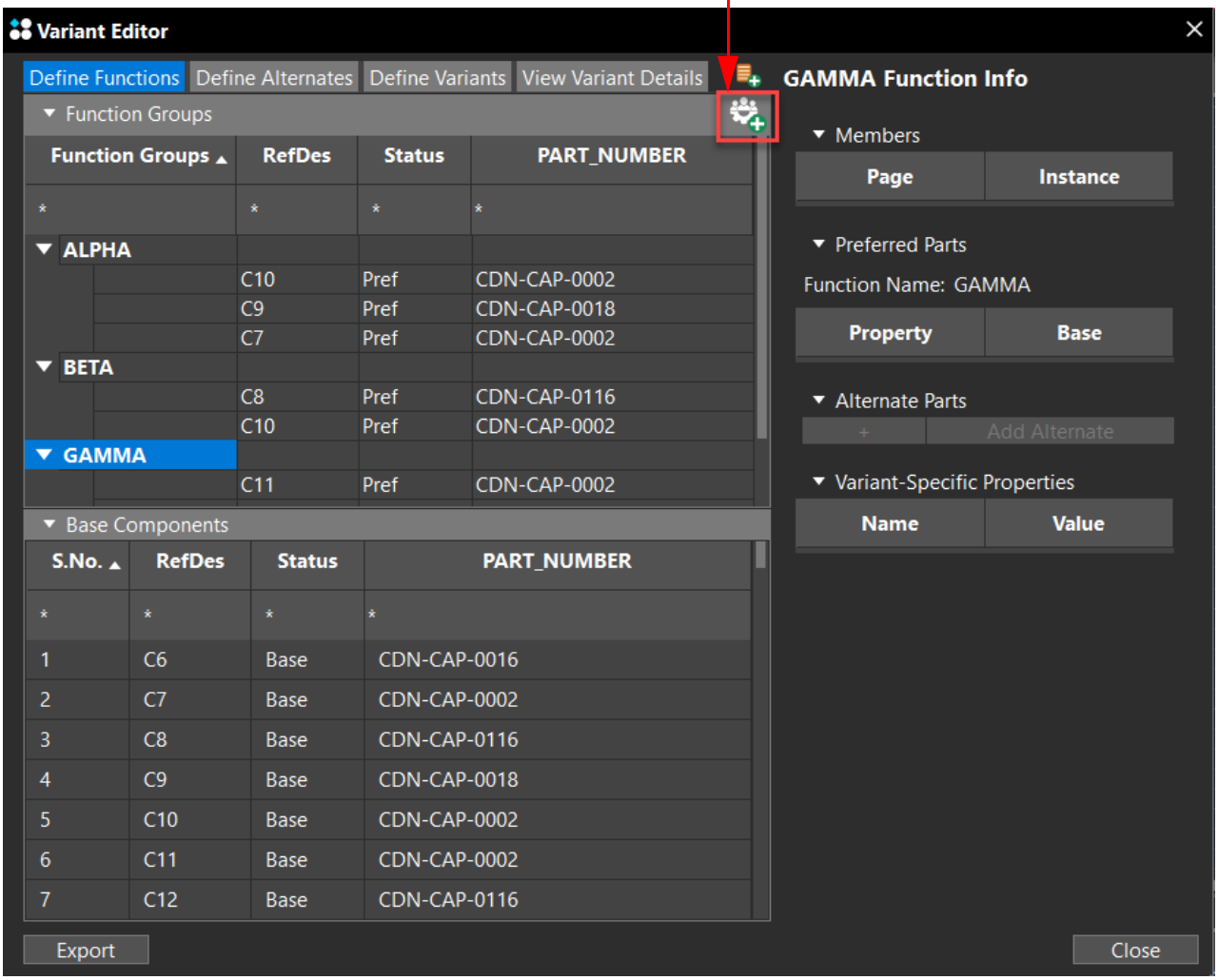
Variant Editor Enhancements

This release has a number of enhancements in Variant Editor. In addition to viewing the variants summary, you can now perform the following tasks:

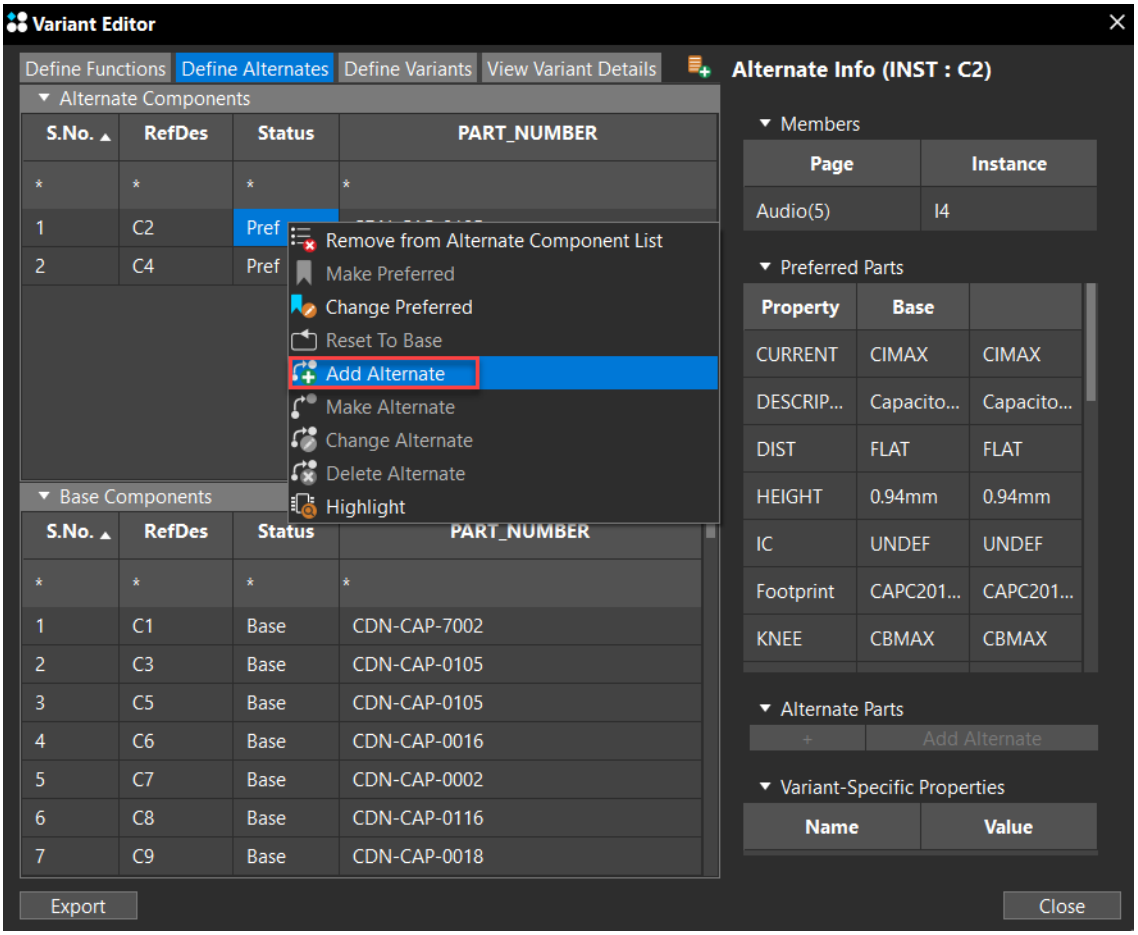
- Create function groups

A function group is a collection of related components that can be added to a variant.

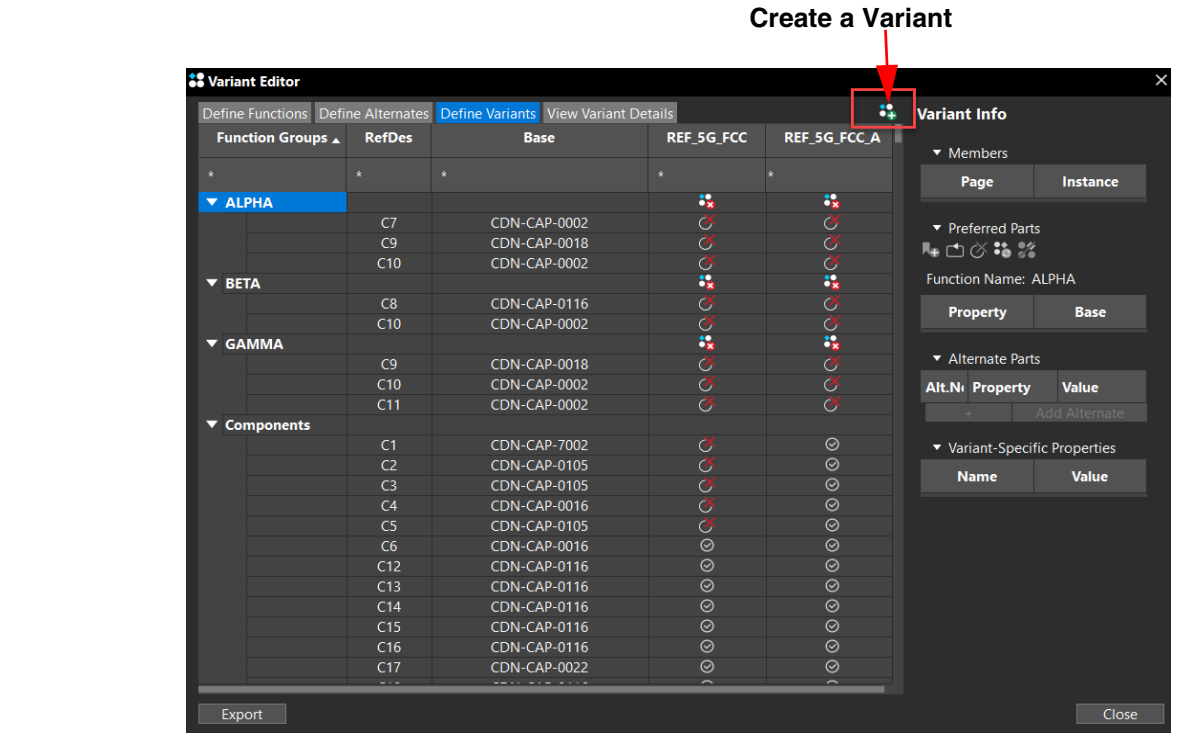
Create a Function Group

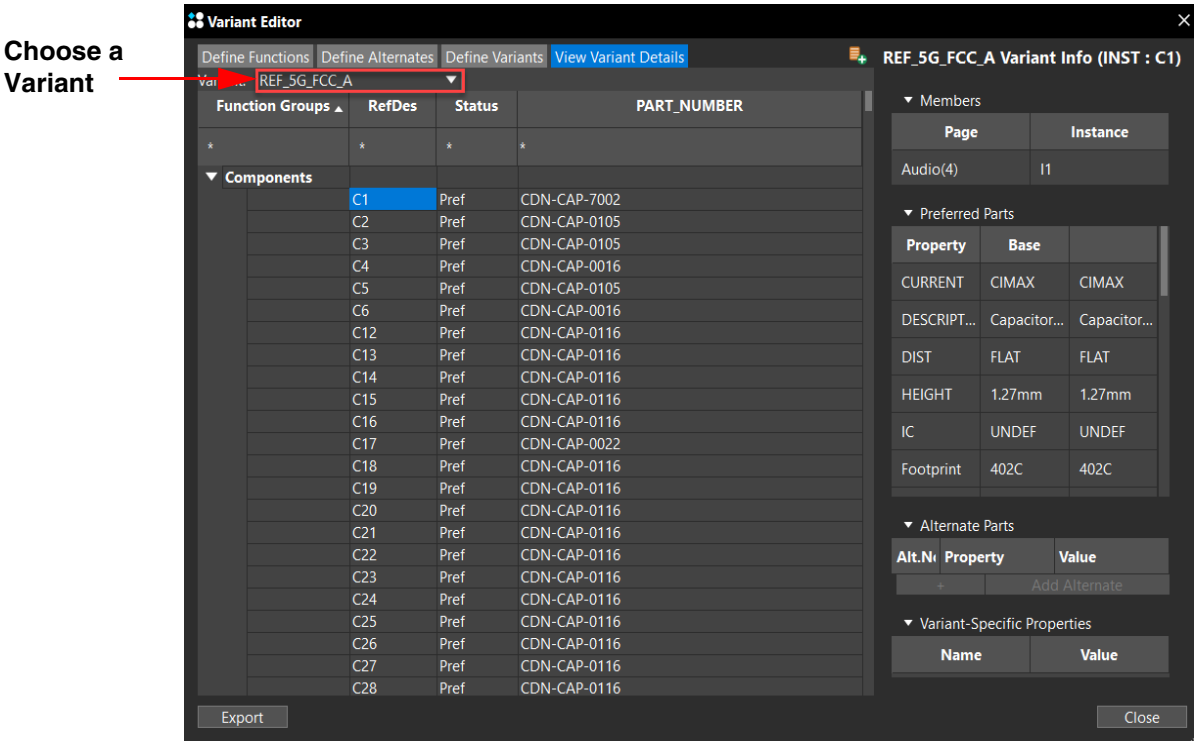


- Define alternate parts



■ Define variants within Variant Editor and switch to a variant to view its details



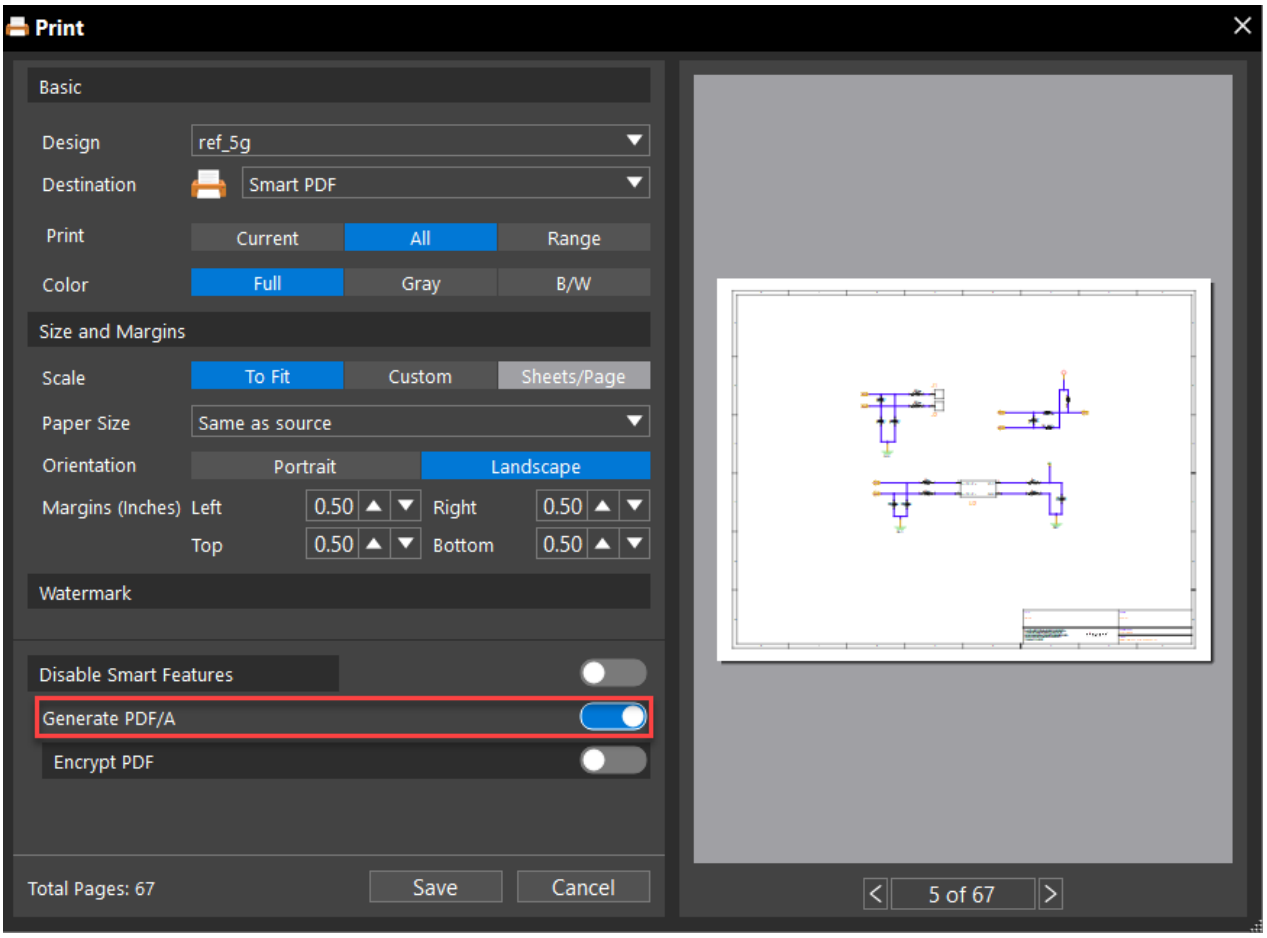


Related Documentation

- Variant Editor

PDF/A Support Added

System Capture now offers long-term archiving ability with the PDF/A format in addition to the PDF and SmartPDF formats.



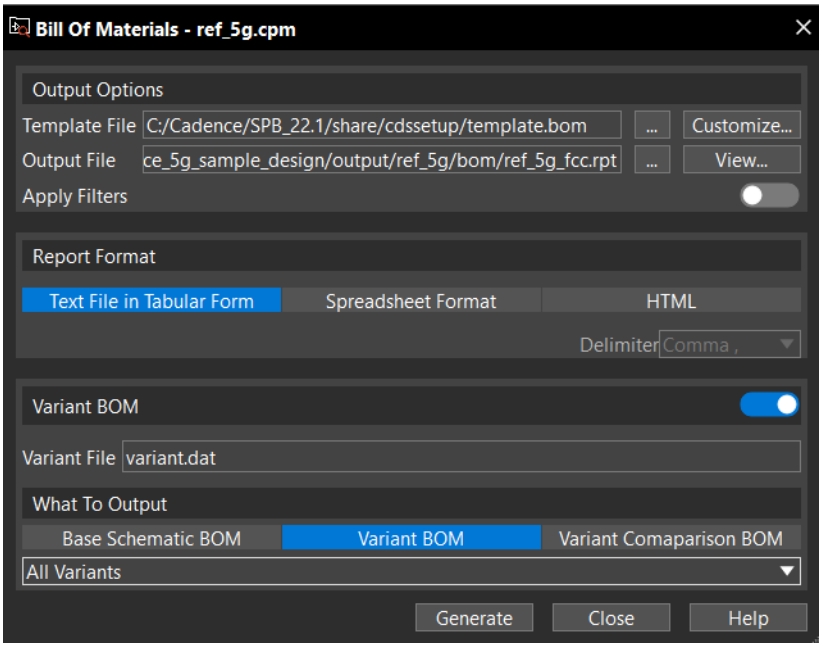
Related Documentation

- Create a PDF

Updated Bill of Materials Dialog Box

The *Bill of Materials* dialog box UI has been updated. Here are some of the changes:

- Radio buttons replaced by tiles
- Check boxes replaced by toggle buttons



Related Documentation

- Using Bill of Materials
- Bill of Materials Dialog box

Documentation Updates

Based on user feedback and to support new enhancements and features, the following guides have substantial changes:

- *Design Integrity and Analysis in Allegro® X System Capture*
- *Allegro® X System Capture User Guide*
- *Allegro System Capture Pulse User Guide* has been renamed to *Design Data Management in Allegro X System Capture*.
- *Allegro System Capture Tcl Commands*

  The following commands have been added or updated

  - `checkIfSyscapUpdateAvailable`
  - `crossprobeInTopology`
  - `dbGetActivePageSpath`
  - `dbGetSPathForActiveTab`
  - `dbSelectObjectById`
  - `downloadAttachment`
  - `dumpMenus`
  - `exportDashboardAsCsv`
  - `exportDashboardAsPdf`
  - `extractPTree`
  - `importBlock`
  - `MTBFPreferences`
  - `newProject`
  - `print`
  - `PTreePreferences`
  - `runMTBFAnalysis`
  - `runThermalAnalysis`
  - `variantEditor`

- `viewThermalMap`

OrCAD X Capture CIS

This section describes the following enhancements and new features in OrCAD® X Capture CIS in release 23.1.

Complete Part Authoring Environment

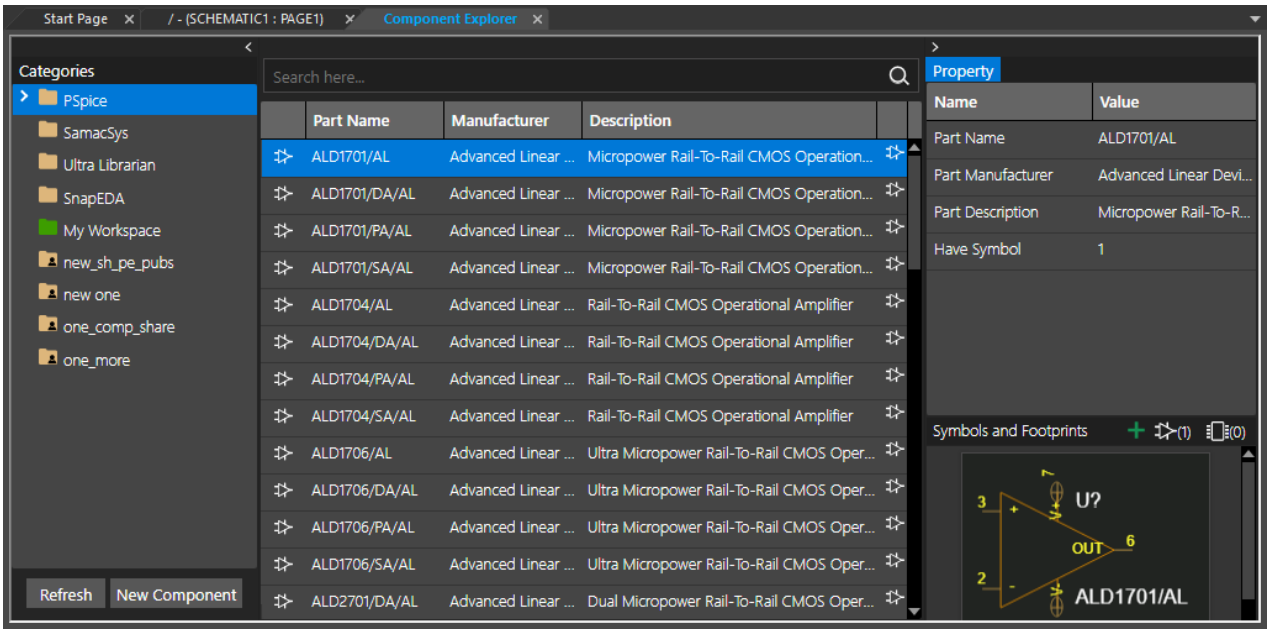
With the `OrCAD X Professional (POX200 Pro)` and `OrCAD X Standard (POX100 Standard)` licenses, you can create new components from scratch or add them from content providers. The complete part authoring solution provides the following functions:

- Place components from content providers in Capture designs
- Search for components in libraries from content providers
- Create a local library of components by adding components from content providers
- Create new components in a local workspace using available symbols, footprints, and PSpice models
- Link a manufacturer part number (MPN) with an existing library component
- Publish components to shared workspaces
- Collaborate with other team members assigning them specific roles

Enhanced Component Explorer

The Component Explorer interface (previously, Unified CIS interface) provides a unified view of all the library sources along with complete part details. The intuitive user interface provides access to various sources including libraries supplied by Cadence and external content

providers. In addition to the PSpice models and associated parts, you can now search, sort, filter, place parts, and create new parts using libraries accessible from OrCAD X Cloud.



Integration with Content Providers

Component Explorer provides access to comprehensive part libraries from content providers to help you build faster designs. Prior to release 23.1, you could access components from SamacSys and Ultra Librarian. Now you can access components provided by SnapEDA as well.

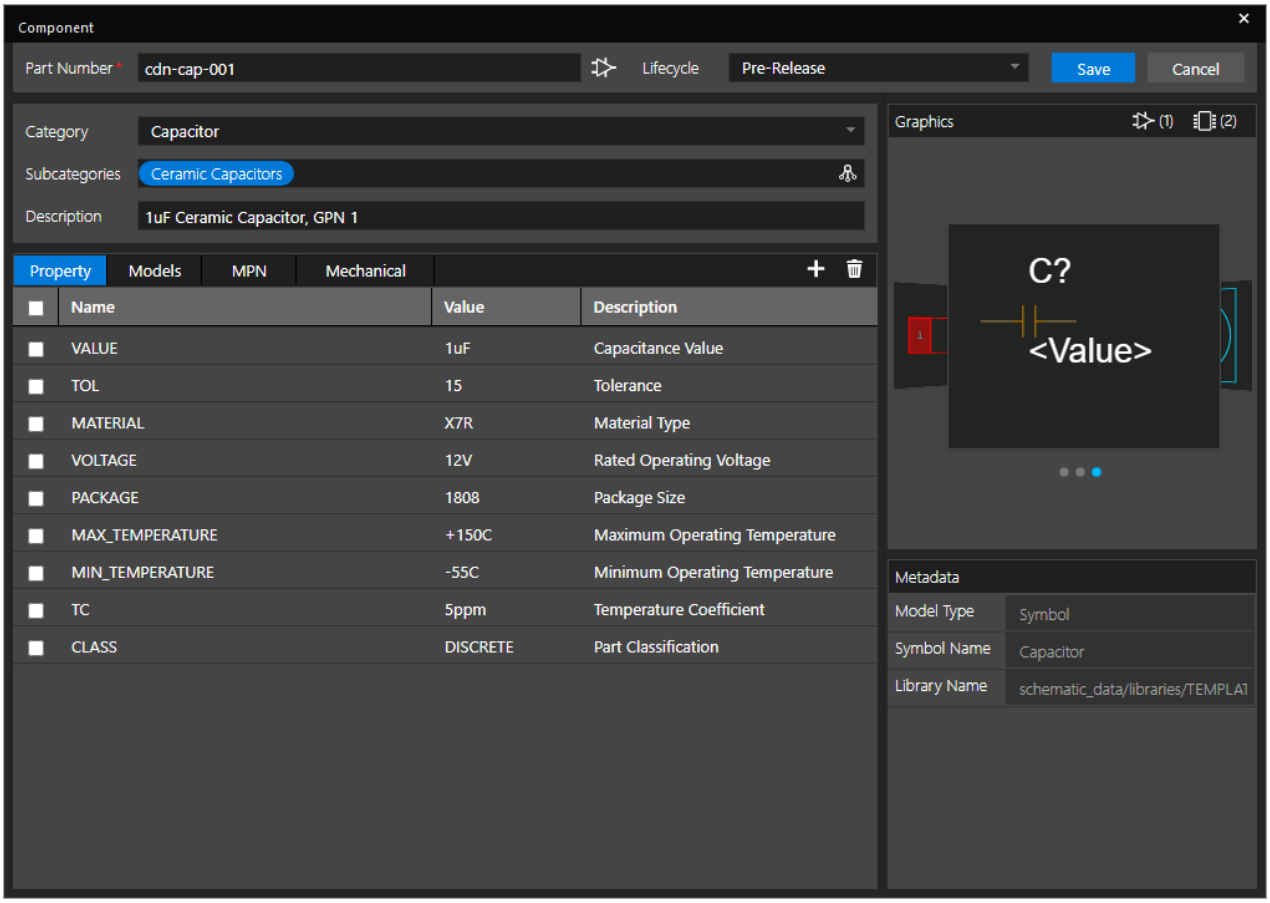
Part Authoring

Capture provides part authoring capability to create new components from scratch using available libraries or from existing parts available from content providers. You create a new component using the *Component* dialog box. From this dialog box, you can:

- Create a new component with:
  - Description
  - Category to organize the part in library database
  - Logical symbol

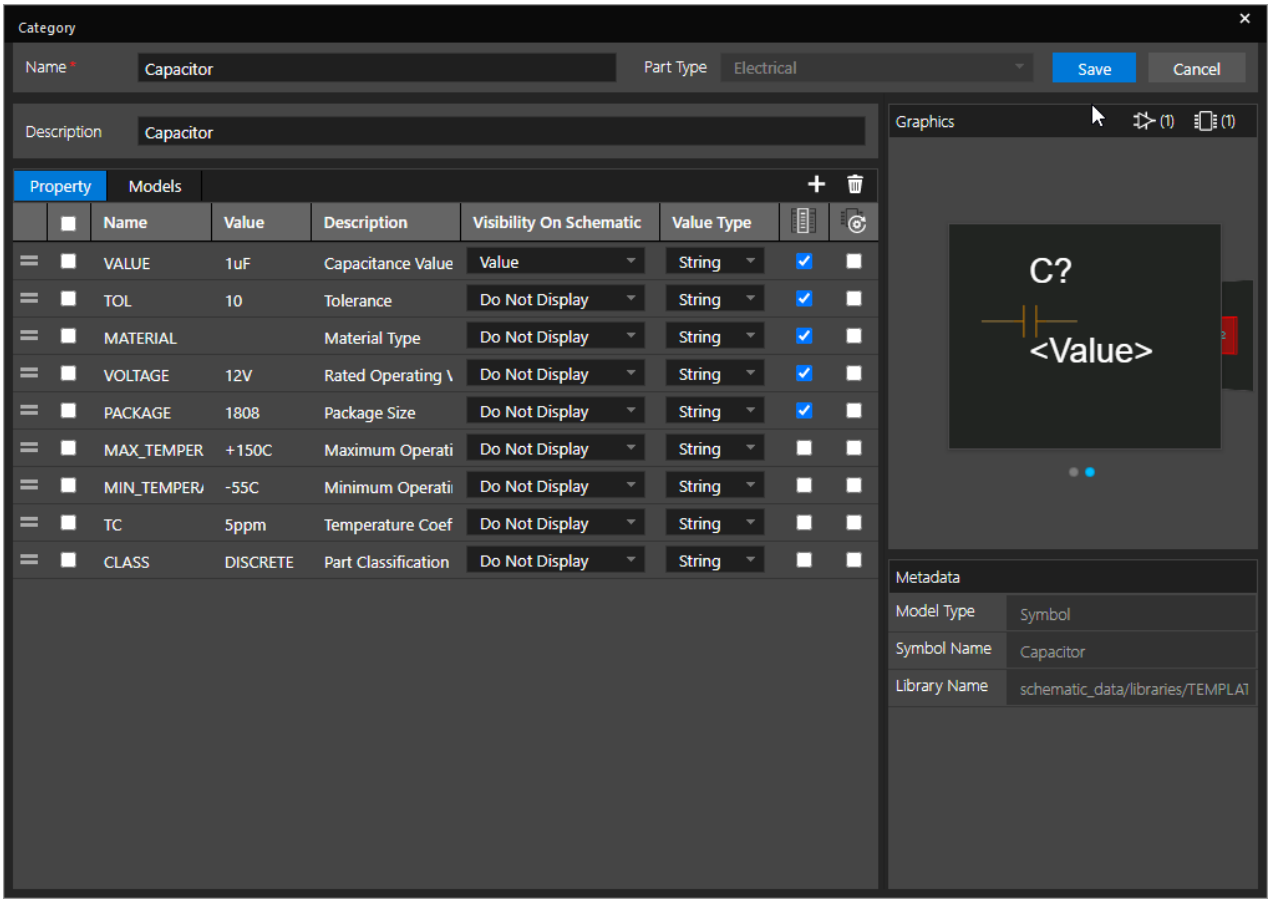
  - Footprint information
  - PSpice models
  - Electrical specification (properties)
- Use existing categories or templates for quick creation of parts with verified symbols, footprints, models, and properties.
- Specify lifecycle status of a component.
- Specify the reuse symbols and footprint information.
- Associate PSpice models and mechanical parts or assemblies.
- Add Manufacturer Part Number (MPN) and associate properties with access to:
  - The latest component data from partners
  - Streamlined library authoring from a single location
- Create a new component from content providers.

- Link the components with manufacturer details provided by the content providers.



Template Creation

A template or category with verified symbols, footprints, models, and properties aids in quick part creation. You can create categories to organize the parts in the workspace (library database).



Related Documentation

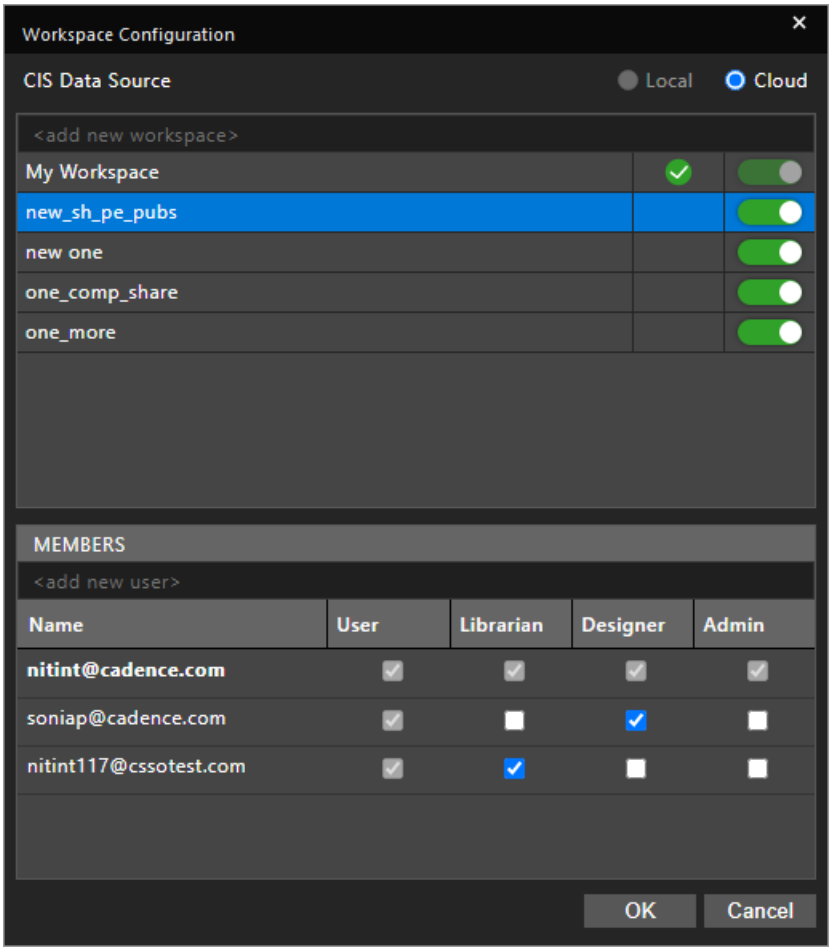
- Creating Components
- Sharing Components
- Component Explorer

Building Team and Workspace

OrCAD X Capture provides a collaborative development environment where you can create shared workspaces containing work-in-progress components, projects, libraries, and design files. A workspace is a Cloud-based project storage location to manage all the library and design data.

You can create multiple workspaces for different projects and user needs, share the workspaces, and provide access rights to team members on shared workspaces by assigning specific roles, such as *User*, *Librarian*, or *Designer*. A member can subscribe to multiple workspaces, have different access privileges (roles) on different workspaces, and move across shared workspaces in the same session of Capture CIS.

Note: The `OrCAD X Professional (POX200 Pro)` license supports creation of up to ten workspaces.



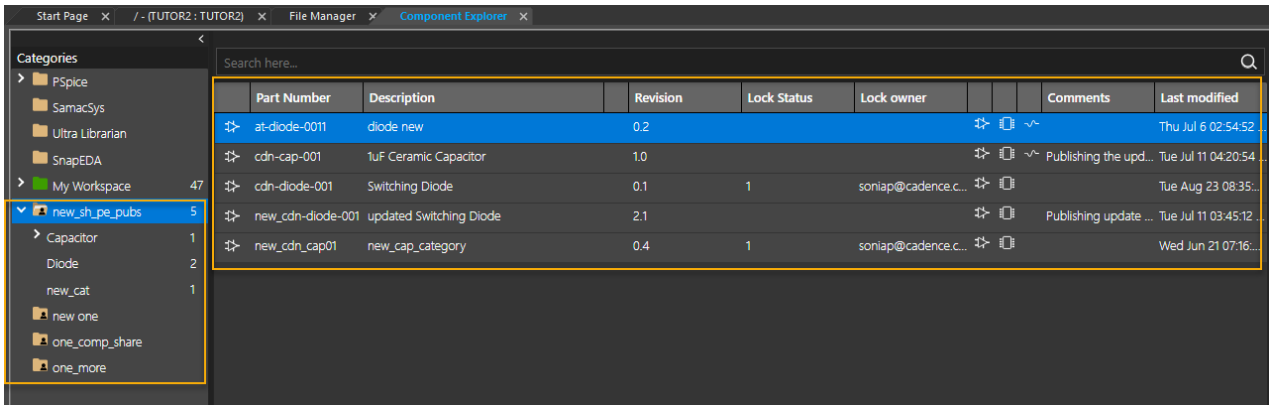
Related Documentation

- Configuring Workspaces
- Sharing Workspaces
- Sharing Projects

Developing Team Component Libraries

The Cloud workspace functionality provides you the capability to create component libraries for your teams by:

- Creating parts in your local workspace (My Workspace)
- Verifying details with part details from the manufacturers
- Creating shared workspaces and assigning specific roles to team members
- Publishing components to shared workspaces



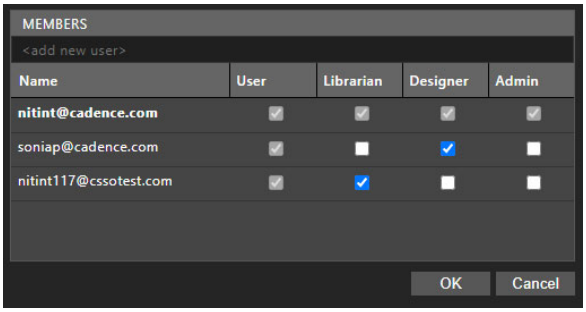
Related Documentation

- Managing a Local Component Library
- Creating Components
- Sharing Components

Library and Design Data Management

You share a workspace to share library and design data including components and design, library, project, and board files with your team members by:

- Creating a shared workspace
- Publishing a library, project, or design files to the shared workspace
- Making the project available to the team members (subscribers)
- Assigning access control in accordance with the roles:
  - *User* can only view the design data.
  - *Designer* can access all design data.
  - *Librarian* can access all library data.
  - *Admin* is the super user who has access to the entire data and can also assign access rights to other users.



A user with access rights can edit or check out the project or a specific file to exclusively work on it.

Related Documentation

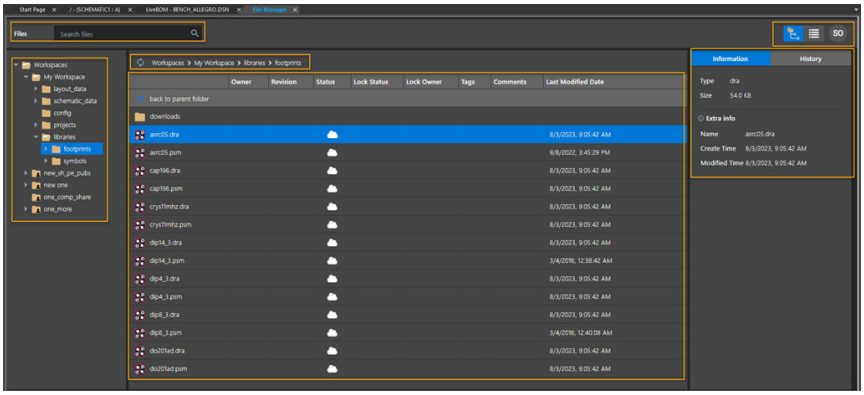
- Managing Libraries on OrCAD X Cloud
- Managing Workspaces

Workspace Content Management

The data in workspace is Cloud enabled and accessible from anywhere. It is always connected to the OrCAD X Cloud, The background data sync utility keeps the data in sync between the local disk and the Cloud.

You manage the libraries, projects, and design files in the workspaces using the File Manager user interface. File Manager displays the local workspace and all the workspaces shared by or with you. A project with its complete folder structure in a workspace is displayed just the way a local project appears in the project manager in Capture. You can perform the following tasks on the workspace content from File Manager:

- View the status of libraries, projects, and design files.
- Edit (check out) and lock libraries, designs, and complete projects to work exclusively on them.
- Publish (check in) files back to the shared workspace.
- View revision history of a file.
- Roll back to a specific revision of a file.

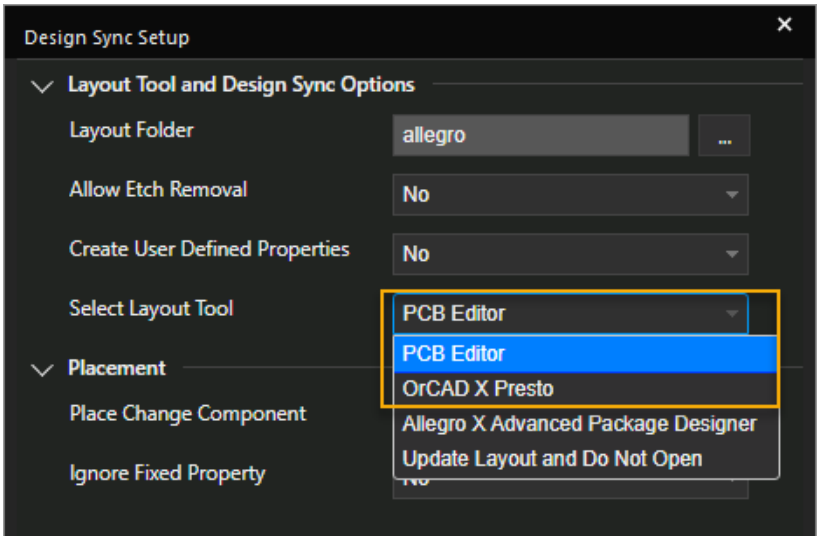


Related Documentation

- Managing Workspaces
- File Manager

Seamless Integration with OrCAD X Presto

The latest PCB layout editor by Cadence, OrCAD X Presto, is fully integrated with Capture CIS. You can perform design synchronization from schematic to PCB and from the PCB to the schematic. You can also cross-probe between the schematic and the layout designs.



Live BOM

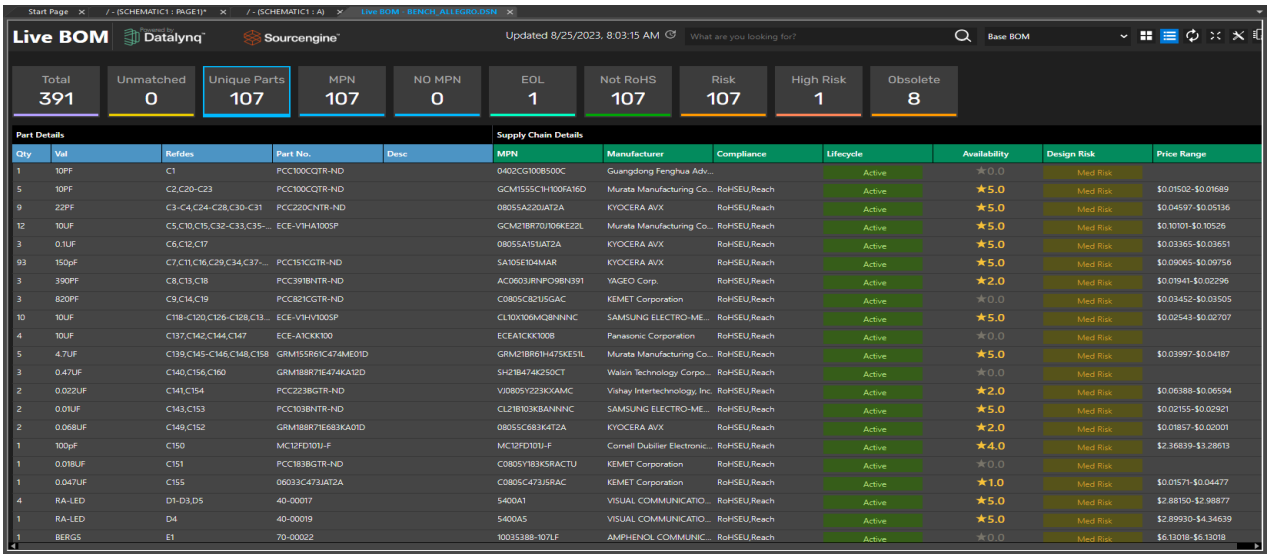
Live BOM is a dynamic bill of materials (BOM) that is generated using supply chain data from SourceEngine. Live BOM represents an always up-to-date view of the design BOM with zero

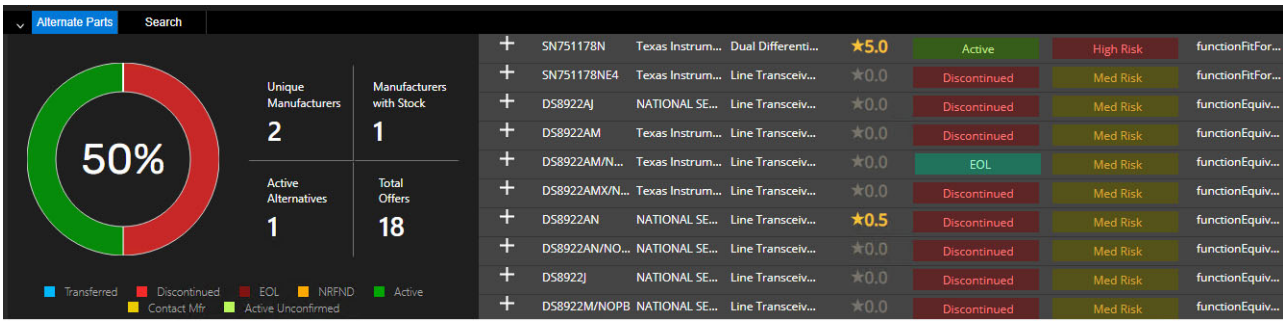
configuration. The rich user Interface provides easy access to the live part status from the Cloud libraries.

The Live BOM feature of Capture CIS supports the following functionality:

- Real-time component availability and price data in the design environment
- Searching and replacing a part with alternative parts
- Viewing alternative parts
- Viewing real time data, cost, availability, and life cycle status of parts in a design
- Dynamic update or on-demand update of the part information
- Global update of the cost and availability data for a design or library
- Support for variant BOM
- Searching, sorting, filtering, and organizing parts in BOM

- Displaying color-coded part rows based on suitability score derived from functional equivalence, life cycle status, and availability





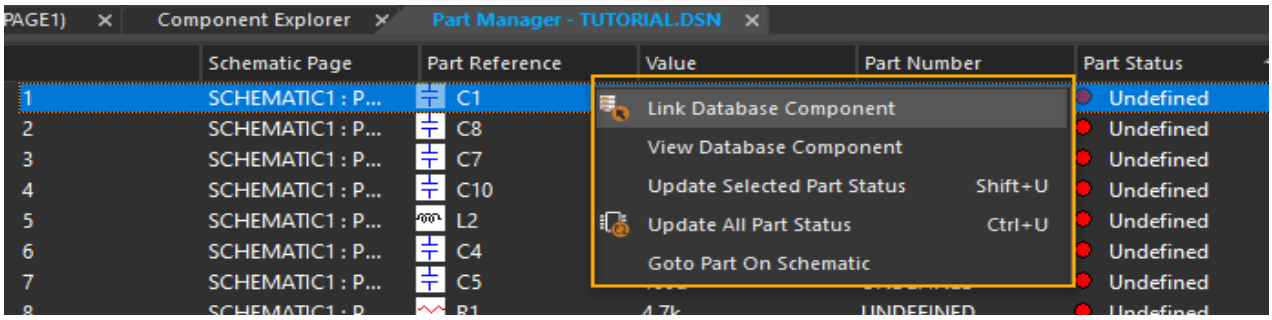
Related Documentation

- Live BOM

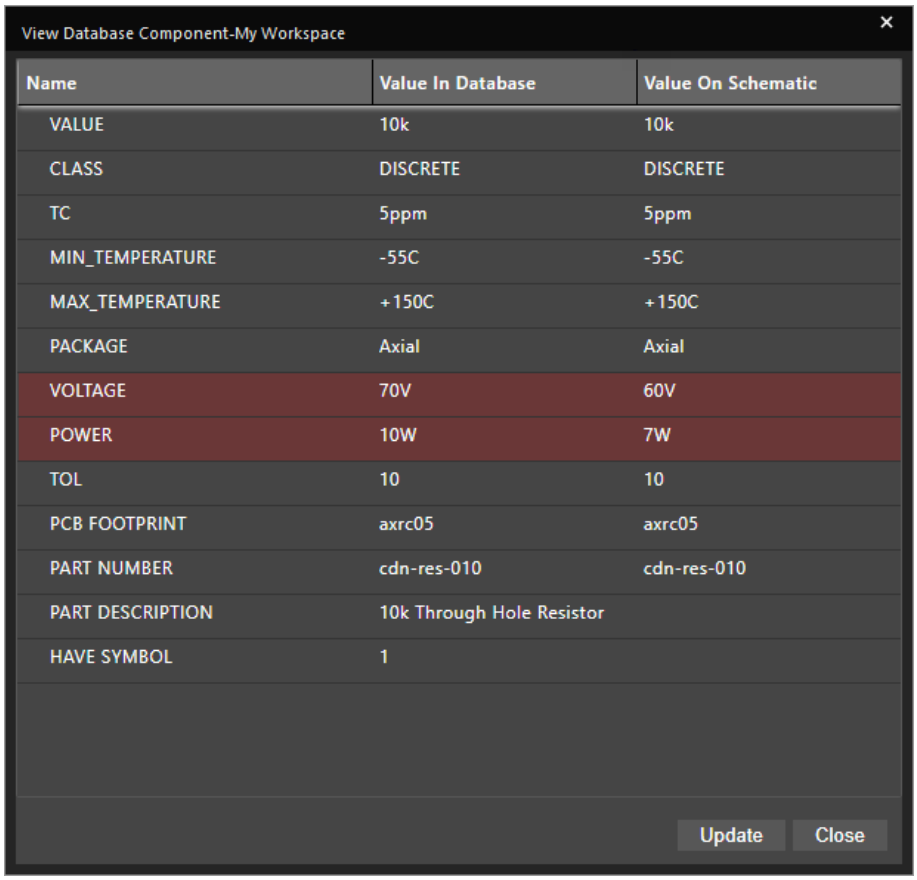
CIS-Specific Features for Cloud CIS

The CIS-specific capability of linking and viewing database parts from the CIS database is extended to the Cloud workspace (database) as well. You can now replace a part instance

and its properties with a workspace component by linking the schematic part to a matching workspace component.



You can also view the part instance with respect to the linked workspace component and sync the two if any differences are found.



Publish for Manufacturing

From OrCAD X Capture, you can quickly and easily publish your design data to a 3D EXPERIENCE PLM server to provide up-to-date design information to various stakeholders. To publish the data to a 3D EXPERIENCE PLM server or the default file system, use the *Tools – Publish for Manufacturing* menu command.

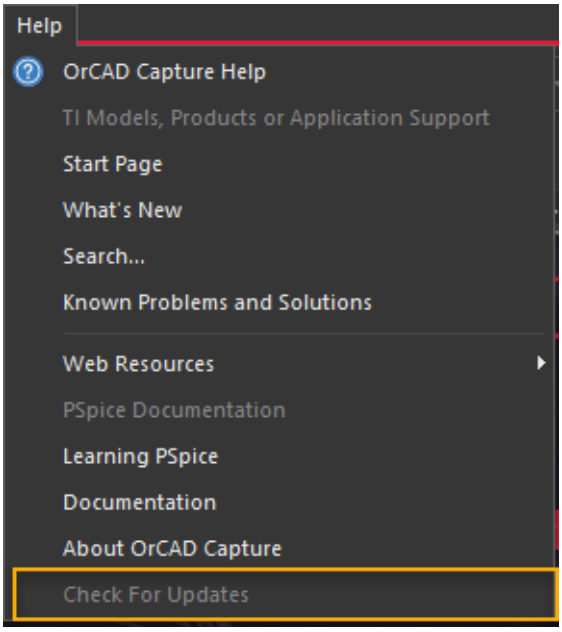
Related Documentation

- *Publish for Manufacturing*

Check for Updates

The Start Page now shows the latest version available for OrCAD X Capture. Click this link to download the newer version.

You can also use *Help – Check For Updates* to check if newer updates are available.



New Documentation

In addition to the new feature documentation, the following new documents are added in release 23.1:

- Library and Part Management in OrCAD X Capture
- OrCAD X Part Authoring Tutorial
- OrCAD X Capture with OrCAD X Presto Tutorial

PSpice and PSpice Advanced Analysis

This section describes the following enhancements and new features in PSpice® and PSpice® Advanced Analysis in release 23.1.

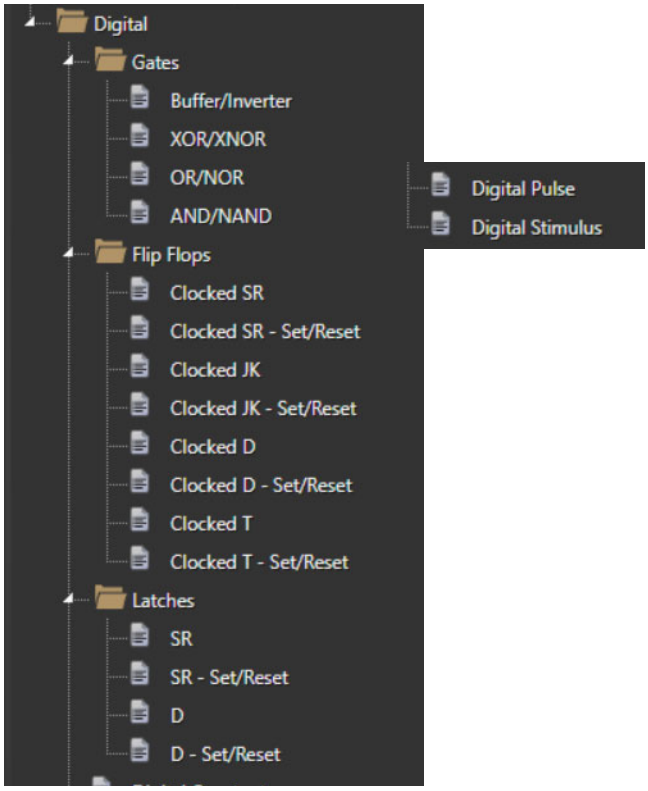
Support for Digital Modeling Application

Release 23.1 supports digital devices and sources in *Modeling Application*. You can model various digital devices such as gates (Buffer, Inverter, AND, OR, and so on), flip flops (Clocked SR, Clocked JK, and so on), latches (SR, D, and so on), and sources (digital stimulus, digital clock) and place them on the schematic.

You can access modeling applications from *Place – PSpice Part* menu in OrCAD X Capture.

The integrated Capture – PSpice flow supports the following digital devices and sources:

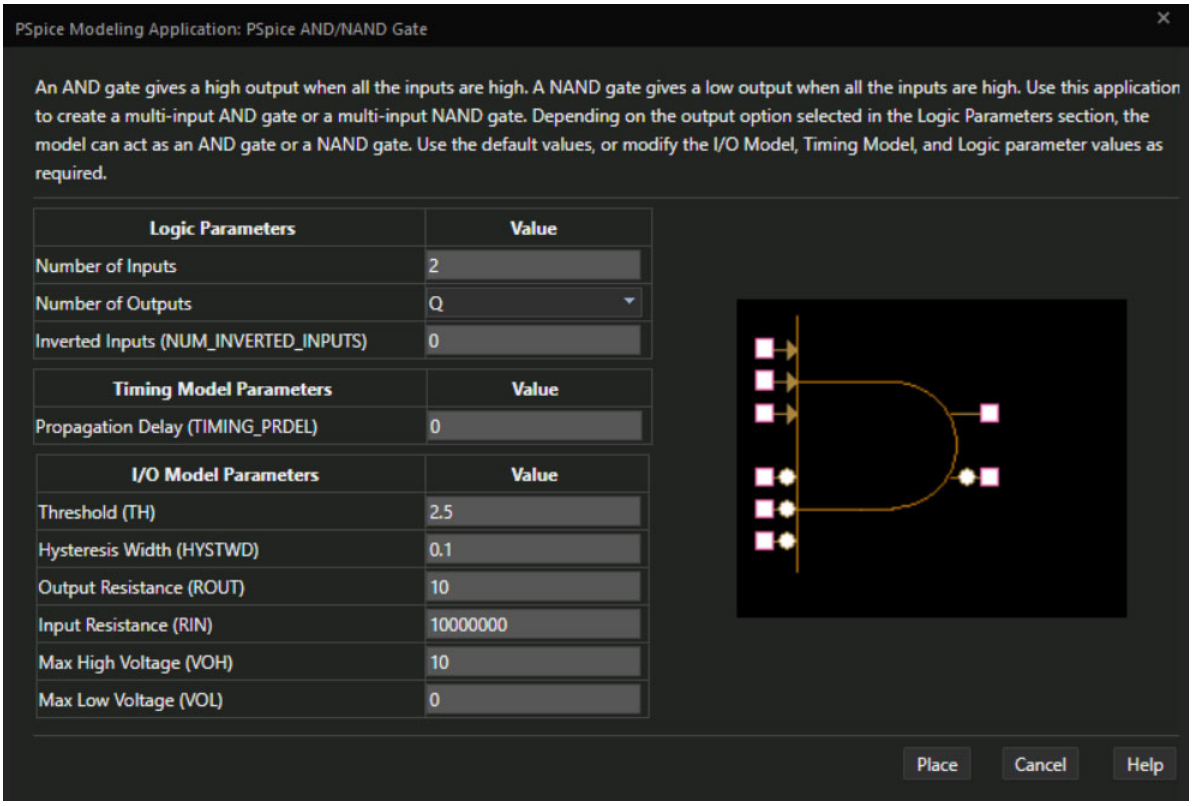
Category	Digital Devices
Sources	Digital Pulse, Digital Stimulus
Gates	Buffer/Inverter, XOR/XNOR, OR/NOR, AND/NAND
Flip Flops	Clocked SR, Clocked SR - Set/Reset, Clocked JK, Clocked JK - Set/Reset, Clocked D, Clocked D - Set/Reset, Clock T, Clocked T- Set/Reset
Latches	SR, SR - Set/Reset, D, D - Set/Reset
	Digital Constant



In release 23.1, digital devices also support logic, timing, and I/O model parameters in *Modeling Application*. You can modify the default values of the parameters before placing the digital devices on the schematic.

- Model logic gates, flip-flops, latches with parameters such as, *Threshold*, *Setup/Hold Time*, *Number of Input/Output*.
- Model digital pulse sources with parameters such as, *Output Resistance (ROUT)*, *Max High/Low Voltage (VOH/VOL)*, *Delay*, and *Clock ON/OFF Time*.

- Model digital stimulus with parameters such as, *Number of Output Nodes*, *Output High/Low Voltage*, and *Output Resistance*.



Temperature Variation in a Single Simulation

PSpice simulator is now enhanced to support temperature that can vary with time in a single transient run. To vary temperature as a function of time in a single run, use an option `.OPTIONS ENABLE_TIME_VARYING_TEMPERATURE`.

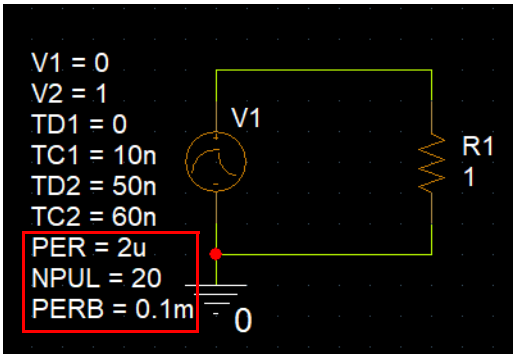
Model parameters such as `T_ABS`, `T_REL_GLOBAL`, and `T_REL_LOCAL` are used for device temperatures for expression in the model definition.

In the expression, use `CDN_CUR_TIME` (alias of time) with temperature-dependent parameters of the components.

Parameter Support for Exponential Sources

To model exponential voltage or a current source, two components, `IEXP_B` and `VEXP_B` are provided in `source.olb`. These components support the following parameters that you can configure, if required:

- `PER`: Defines pulse period.
- `NPUL`: Defines the number of pulse.
- `PERB`: Defines the repeat burst period.



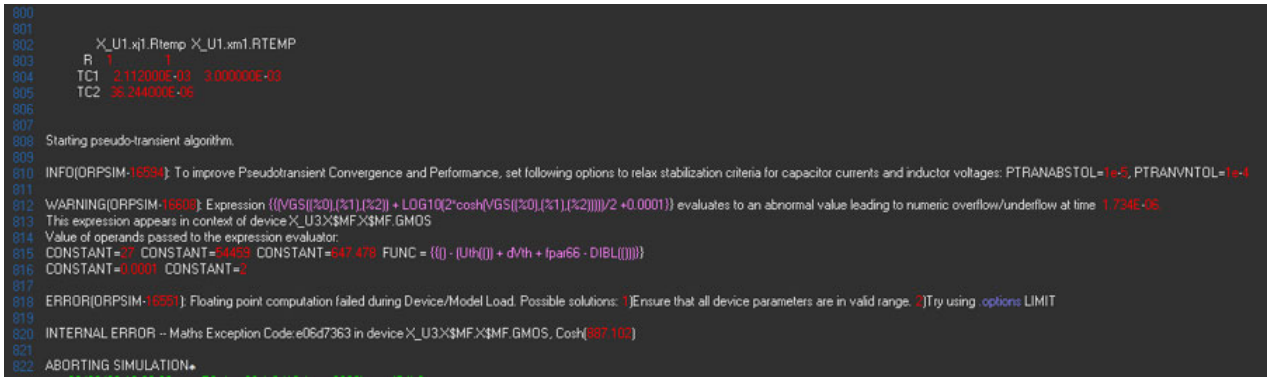
Enhanced Debugging of Convergence Error

Abnormal high or low values or floating point errors in complex circuits often lead to convergence errors. However, it is difficult to find the exact expression that causes the error.

As an enhancement in the 23.1 release, you can now use the EXPR_DEBUG option to include the expressions in the warning message that cause convergence errors.

Syntax to use the option: `.OPTIONS EXPR_DEBUG`.

The following image shows a warning message (ORPSIM-16608) that lists the expression leading to the convergence error.



Sigrity Aurora

This section describes the following enhancements and new features in Sigrity™ Aurora in release 23.1.

New XtractIM Workflow in Aurora for Allegro Advanced Package Designer

A new workflow, *XtractIM Workflow*, is added for Allegro® X Advanced Package Designer (APD) only. This workflow allows quick package design parasitics analysis. The following two types of simulation/analysis are supported in the XtractIM workflow:

- Per Pin (Die-side Power)
  - Quickly identifies die power/ground quality corner cases
  - Reports resistance, self inductance, total inductance
- Per Net (Signal)
  - Produces R, L, C, Delay, and Lengths for each selected net

Aurora visions overlay for all the results categories. High-performance computing is supported in the workflow for accelerated results.

Existing Workflows Now Available in Allegro Advanced Package Designer

The following workflows that are already available in Allegro X PCB Editor and Aurora are now supported in Allegro X Advanced Package Designer (APD):

- Power Inductance Workflow
- Topology Extraction Workflow

Power Inductance Workflow

This workflow allows analysis of capacitor-to-IC and IC power pin parasitics. HTML reports can be generated.

Topology Extraction Workflow

This workflow allows you to extract interconnect to Topology Workbench for examination and time-domain simulation.

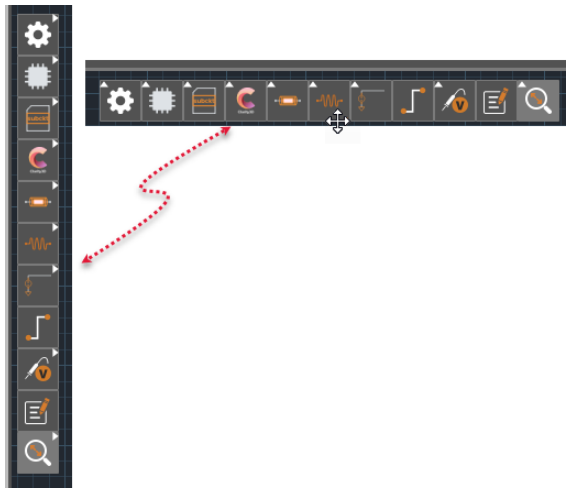
Topology Workbench

This section describes the following enhancements and new features in Topology Workbench in release 23.1.

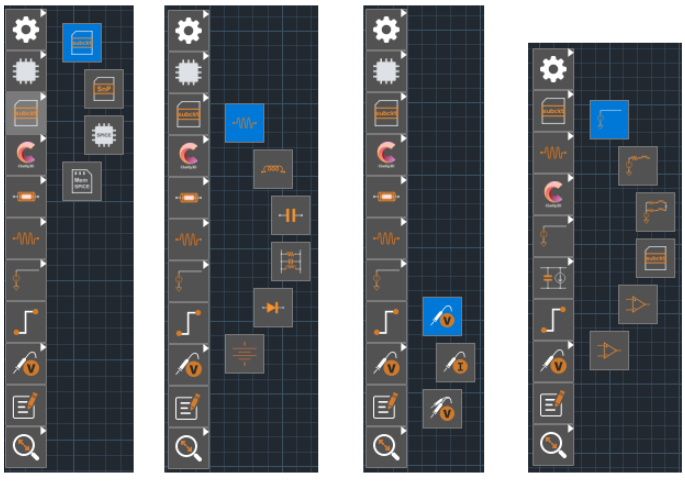
Common Update

Floating Toolbar Replaces the Add Block Panel and Features New Block Icons

Starting this release, the Add Block panel has been removed. Instead, a new floating toolbar is available in the main application window with controls to help with various design operations on the canvas. It is by default aligned vertically and can be docked horizontally per convenience.



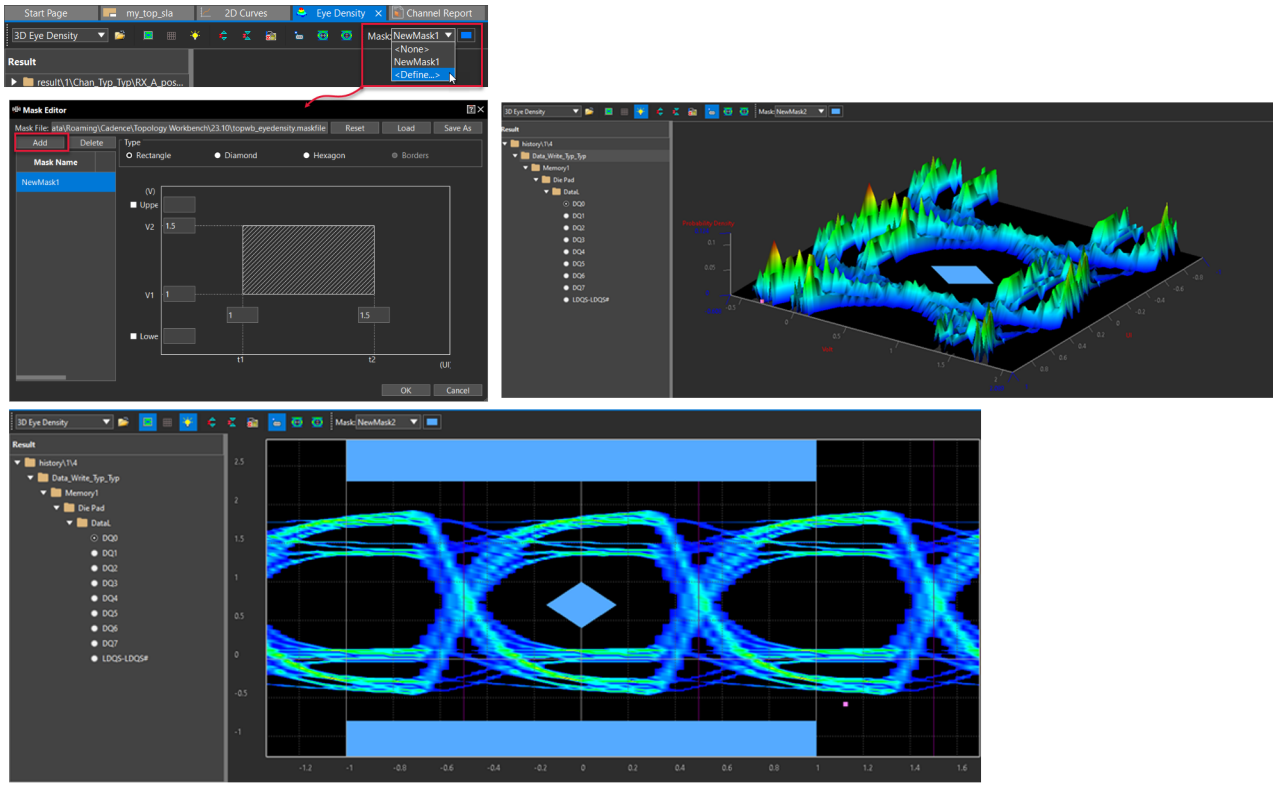
The floating toolbar features improved icons for placing blocks on the canvas. Only a subset of icons is visible at a time. To explore the additional blocks that can be added to the canvas, right-click any of the icons in the floating toolbar.



SystemSI Updates

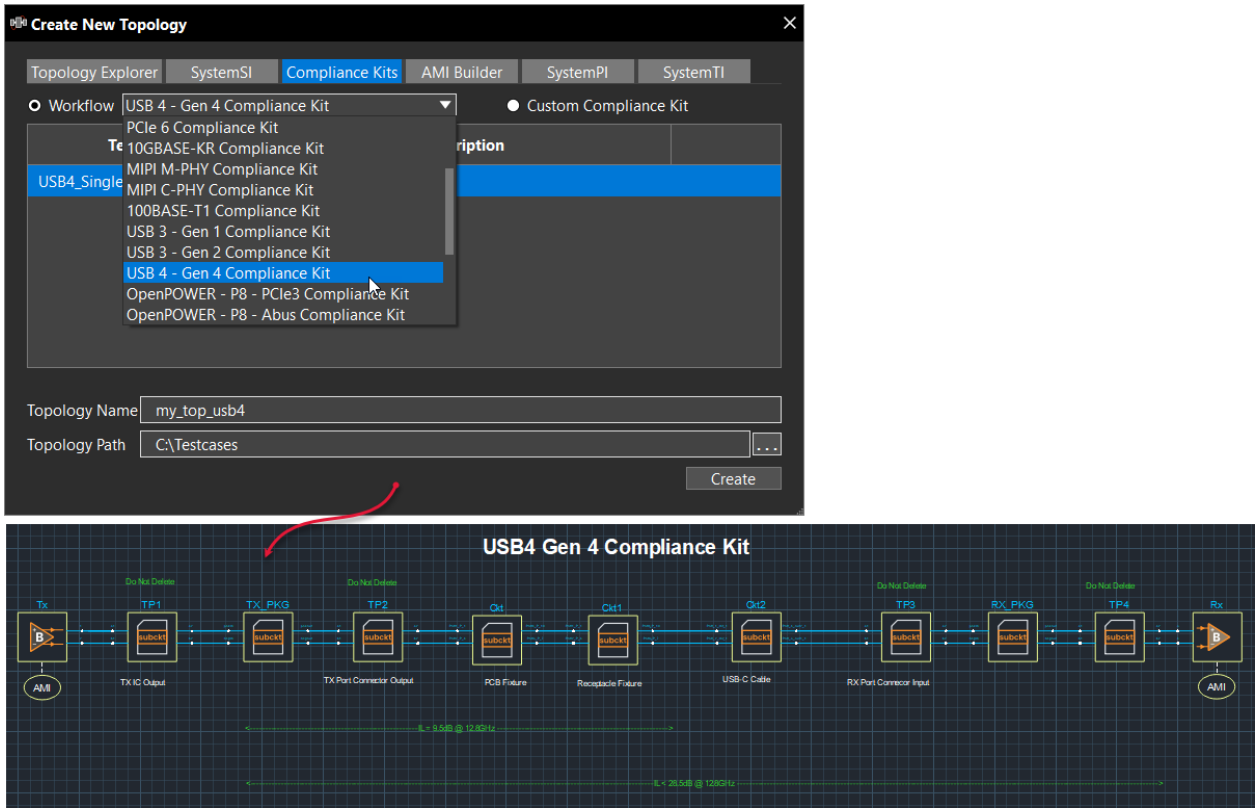
Eye Mask Support Added to 3D Eye Density Plots

On completion of a channel simulation run in the Parallel Bus Analysis (PBA) or Serial Link Analysis (SLA) workflow, you can now define and apply eye mask values to the 3D plots in the Eye Density tab.



USB4 Gen 4 Compliance Kit Supported

The Compliance Kits workflow now supports USB 4 - Gen 4 Compliance Kit. With this enhancement, you can run PAM3 simulation at a defined Baud Rate for a single lane topology comprising Tx, Rx, Tx and Rx Port Connectors, PKG, Cable, and fixtures.



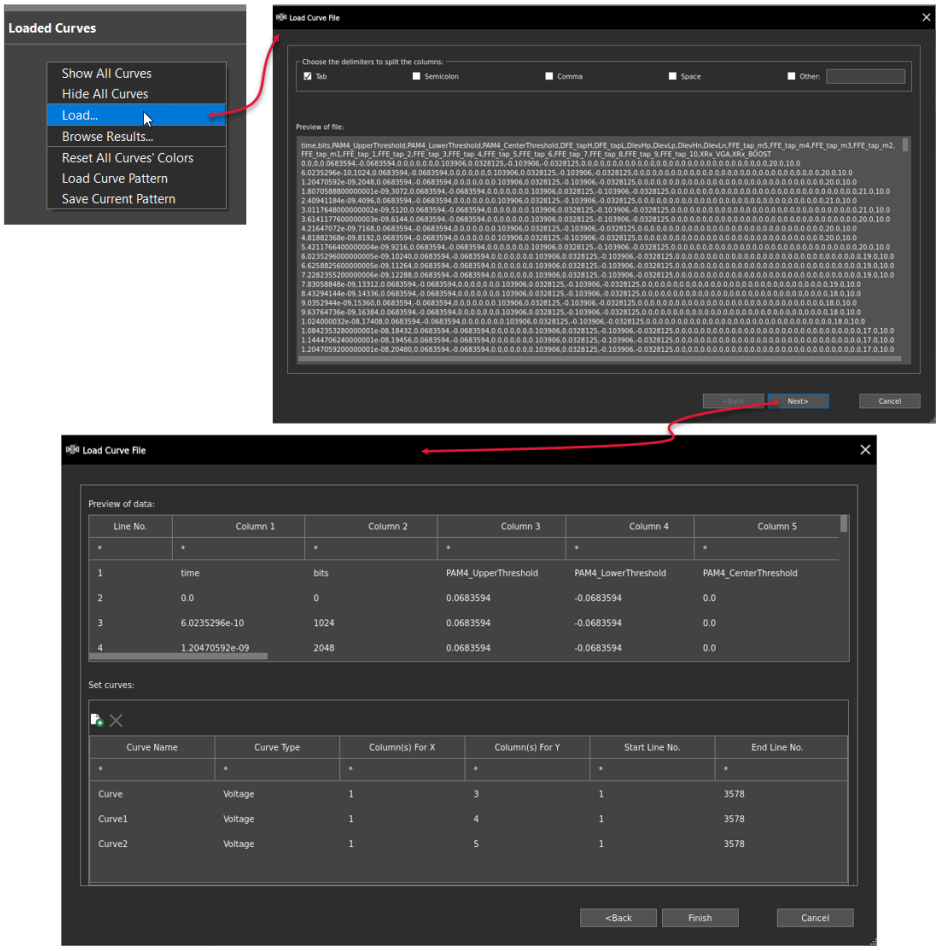
The related compliance items include the transmitter and receiver tests for parameters such as:

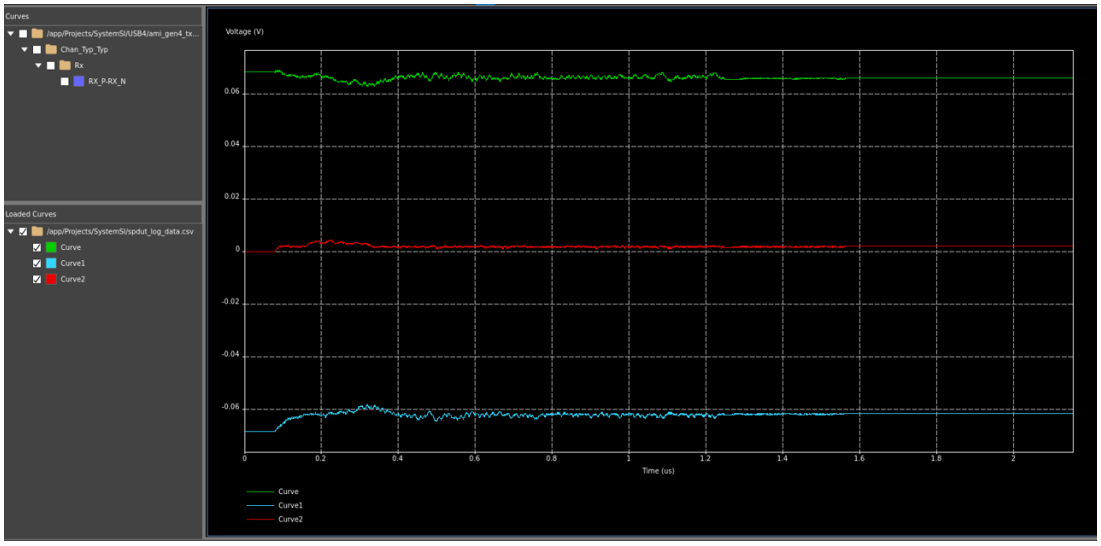
- Tx level, Tx differential return loss, and Tx signal to noise distortion ratio (SNDR) (Section 3.2.3.4)
- Rx end-to-end channel differential insertion loss, Rx differential return loss, and Rx tolerance test (Section 3.2.4.2)

Except for a few components labeled as *Do Not Delete*, you can replace workspace items in the single lane topology with your own design models. The compliance report is generated on completion of the checks.

Import CSV Data into Waveform Display

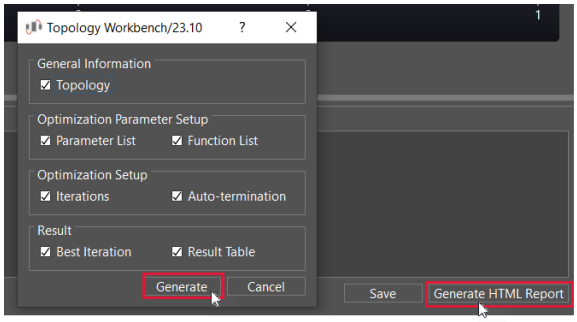
Some AMI models write data to a CSV file for post-processing and analysis. This data can now be imported and displayed in the 2D Curves tab with the simulation results.





Optimality Interface Enhanced to Generate a Report

In this release, the *Generate HTML Report* button has been added to the Optimality window for Topology Workbench. Clicking this button opens a dialog box that lets you configure the contents of the report and generate the Topology Workbench Optimality Report.



2 Optimization Parameter Setup

2.1 Parameter List

Index	Optimize	Name	Type	Expression	Ref Value	Unit	BoundType	LowBound	HighBound	Step	Array
1	True	Trace_W	continous	1mm	1	mm	relative	1	2		
2	False	Trace_R	continous	2mm	2	mm	relative				

Return to Top

2.2 Function table

Name	Mode	Expression	Custom Function	Type	Indexi	Indexj	Target
obj		E12		Objective Function(goal)			
E12	single_end			Average	1	2	

4 Result

4.1 Best Iteration

Best Iteration: 5

Return to Top

4.2 Result Table

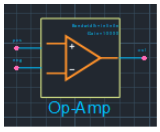
Index	obj	E12	Trace_W
0	0.999261	0.999261	1.23412
1	0.978154	0.978151	1.54421
2	0.951231	0.951231	1.1325
3	0.983121	0.983121	1.32489
4	0.977281	0.977281	1.525494
5	0.923211	0.923211	1.85421

SystemPI Update

Support Added for New VRM Models

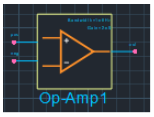
The following two operational amplifier (Op-Amp) blocks have been added to model voltage regulator modules (VRM) more accurately:

- *Ideal Op-Amp*, which is a model having a simple voltage-controlled voltage source (VCVS) with an input impedance resistor and output impedance resistor.



Name	Value
Block Name	Op-Amp
Input Impedance	1e7Ohm
Gain	10000
Output Impedance	0.1 Ohm

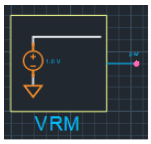
- *Bandwidth-Limited Op-Amp*, which is a model having an ideal op-amp with a bandwidth limit.



Name	Value
Block Name	Op-Amp1
Input Impedance	2e6Ohm
Gain	2e5
Bandwidth	1e6Hz
Output Impedance	0.1 Ohm

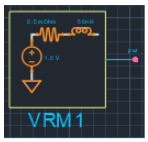
In addition, the following VRM blocks have been updated:

- *Ideal Supply (VDC) VRM*, which is a simple DC model.



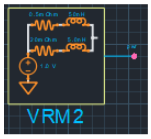
Name	Value
Block Name	VRM
Nominal Voltage	1.0 V
▼ Power Net	
Net Name	PWR
# of Pins	1
Pin Name	pwr
Pin Resistance(Ohm)	0
▶ Ground Net	

- *RL VRM*, which is a 2-element model having a VDC source with a series resistor (R) and an inductor (L).



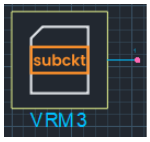
Name	Value
Block Name	VRM1
Nominal Voltage	1.0 V
▼ Power Net	
Net Name	PWR
# of Pins	1
Pin Name	pwr
R_VRM(Ohm)	0.5m
L_VRM(H)	50n
▶ Ground Net	

- *RL//RL VRM*, which is a 4-element model having a VDC source with a parallel combination of the series resistor and inductor as in the 2-element model.



Name	Value
Block Name	VRM2
Nominal Voltage	1.0 V
▼ Power Net	
Net Name	PWR
# of Pins	1
Pin Name	pwr
R_VRM(Ohm)	0.5m
L_VRM(H)	50n
R_damp(Ohm)	20m
L_VRM/10(H)	5.0n
▶ Ground Net	

- *Subckt VRM*, which is a subcircuit model based on a user-supplied netlist model for a VRM model.



Name	Value
Block Name	VRM3
Circuit File	vrm_Smith.sp